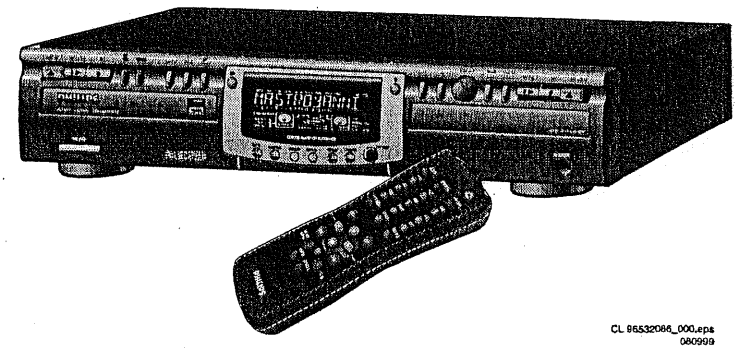
Compact disc recorder

CDR775

/00

Service
Service
Service



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Service Manual

SERVICING

For servicing CDR775, the set can divided into three parts.

1. The display board (partly) 1 002, the I/O board 1004, the headphone board (partly) 1002, the IR board (partly) 1002, the ON/ OFF & Standby LED board (partly) 1002 and the CD-out board (partly) 1002 have to be repaired at component level. The power supply unit 1003 is available as spare part, but can also be repaired at component level.
2. The CDR module (containing the CDR loader 81, CDR main board 1001 and loader bracket 82, 83) will be exchanged completely in case of failure. This complete CDR module is available as spare part. Defective modules have to be returned for central repair.
3. The CD module (containing the CD loader 131, CD main board 1005 and loader bracket 132) is a new module with VAL1250 loader assy but also a separate CDM and separate loader parts will be available via service stock. The CD main board can be repaired at component level.

Also available: Circuit Description " The Basics of Compact Disc Recordable/Rewriteable". Service code number 4822 725 25242.

Contents

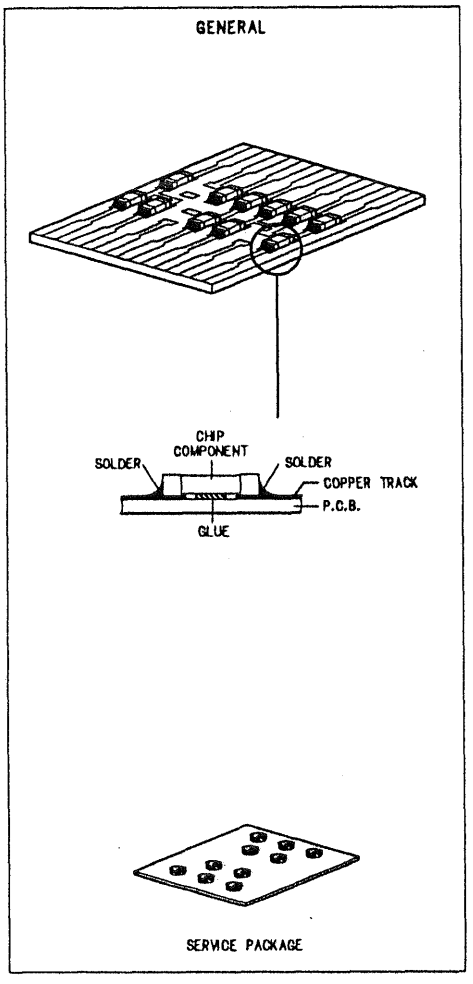
CLASS 1
LASER PRODUCT

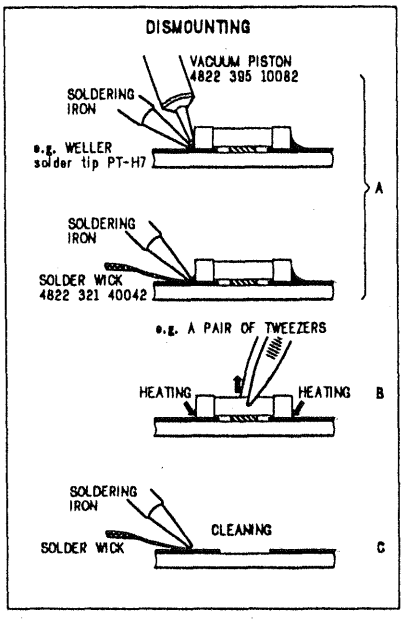
Published by RH 9969 Service DPS Hasselt Printed in the Netherlands Subject to modification GB 3104 125 40030

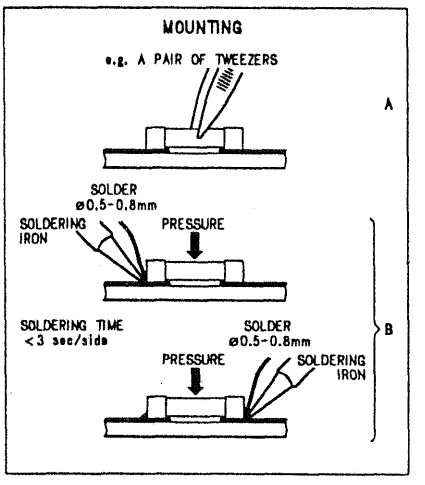
PHILIPS

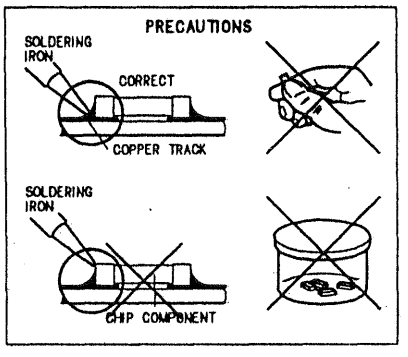
SERVICING HINTS

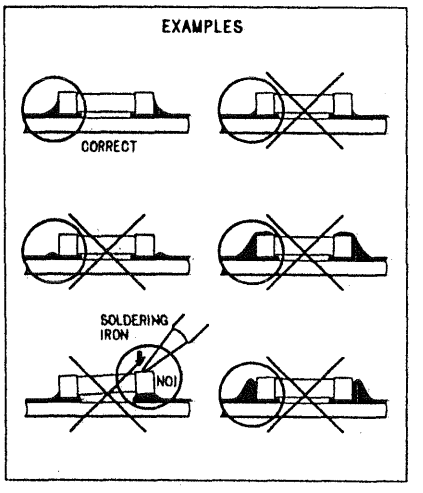
In the set, chip components have been applied. For disassembly and assembly check the figure below.











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SAFETY GUIDELINES FOR THE PROFESSIONAL SERVICE TECHNICIAN

Important

Proper service and repair is important to the safe, reliable operation of all Philips equipment. The service procedures recommended by Philips and described in this service manual are effective methods of performing service operations. Some of these service operations require the use of tools specially designed for the purpose. The special tools should be used when and as recommended.

It is important to note that this manual contains various CAUTIONS and NOTICES which should be carefully read in order to minimize the risk of personal injury to service personnel. The possibility exists that improper service methods may damage the equipment. It also is important to understand that these CAUTIONS and NOTICES ARE NOT EXHAUSTIVE. Philips could not possibly know, evaluate and advise the service trade of all conceivable ways in which service might be done or of the possible hazardous consequences of each way. Consequently, Philips has not undertaken any such broad evaluation. Accordingly, a servicer who uses a service procedure or tool which is not recommended by Philips must first satisfy himself thoroughly that neither his safety nor the safe operation of the equipment will be jeopardized by the service method selected.

Safety Checks

After the original service problem has been corrected, a complete safety check should be made. Be sure to check over the entire set, not just the areas where you have worked. Some previous servicer may have left an unsafe condition, which could be unknowingly passed on to your customer. Be sure to check all of the following:

Fire and Shock Hazard

1. Be sure all components are positioned in such a way as to avoid the possibility of adjacent component shorts. This is especially important on those units which are transported to and from the service shop.
2. Never release a repaired unit unless all protective devices such as insulators, barriers, covers, strain reliefs, and other hardware have been installed according to the original design.
3. Soldering and wiring must be inspected to locate possible cold solder joints, solder splashes, sharp solder points, frayed leads, pinched leads, or damaged insulation (including the ac cord). Be certain to remove loose solder balls and all other loose foreign particles.
4. Check across-the-line components and other components for physical evidence of damage or deterioration and replace if necessary. Follow original layout, lead length, and dress.
5. No lead or component should touch a resistor rated at 1 watt or more. Lead tension around protruding metal surfaces or edges must be avoided.
6. Critical components having special safety characteristics are identified with a ⚠ by the Ref. No. in the parts list and enclosed within a broken line* (where several critical components are grouped in one area) along with the safety symbol ⚠ on the schematic diagrams and/or exploded views.

   Replacement parts without the same safety characteristics may create shock, fire, or other hazards.
7. When servicing any unit, always use a separate isolation transformer for the chassis. Failure to use a separate isolation transformer may expose you to possible shock hazard, and may cause damage to servicing instruments.
8. Many electronic products use a polarized ac line cord (one wide pin on the plug). Defeating this safety feature may create a potential hazard to the servicer and the user. Extension cords which do not incorporate the polarizing feature should never be used.

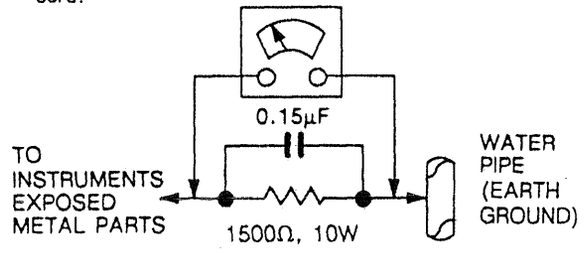
Fire and Shock Hazard (Continued)

9. After reassembly of the unit, always perform an ac leakage test or resistance test from the line cord to all exposed metal parts of the cabinet. Also, check all metal control shafts (with knobs removed), antenna terminals, handles, screws, etc. to be sure the unit is safe to operate without danger of electrical shock.

* Broken line: ▬ ▪ ▬ ▪ ▬ ▪ ▬ ▪ ▬

Leakage Current Cold Check

1. Unplug the ac line cord and connect a jumper between the two prongs of the plug.
2. Turn on the power switch.
3. Measure the resistance value between the jumpered ac plug and all exposed cabinet parts of the receiver, such as screw heads, antennas, and control shafts. When the exposed metallic part has a return path to the chassis, the reading should be between 1 megohm and 5.2 megohms. When the exposed metal does not have a return path to the chassis, the reading must be infinity. Remove the jumper from the ac line cord.



Leakage Current Hot Check

1. Do not use an isolation transformer for this test. Plug the completely reassembled unit directly into the ac outlet.
2. Connect a 1.5k, 10W resistor paralleled by a 0.15uF. capacitor between each exposed metallic cabinet part and a good earth ground such as a water pipe, as shown above.
3. Use an ac voltmeter with at least 5000 ohms/volt sensitivity to measure the potential across the resistor.
4. The potential at any point should not exceed 0.75 volts. A leakage current tester may be used to make this test; leakage current must not exceed 0.5 milliamps. If a measurement is outside of the specified limits, there is a possibility of shock hazard. The receiver should be repaired and rechecked before returning it to the customer.
5. Repeat the above procedure with the ac plug reversed. (Note: An ac adapter is necessary when a polarized plug is used. Do not defeat the polarizing feature of the plug.)

Parts Replacement

1. Many electrical and mechanical parts in Philips equipment have special safety related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. The use of a substitute part which does not have the same safety characteristics as the Philips recommended replacement part shown in this service manual may create shock, fire, or other hazards. Under no circumstances should the original design be modified or altered without written permission from Philips. Philips assumes no liability, express or implied, arising out of any unauthorized modification of design. Servicer assumes all liability.
2. All ICs and many other semiconductor parts are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce the life of the part drastically.

LASER NOTE:

DANGER - Invisible laser radiation when open. AVOID DIRECT EXPOSURE TO BEAM.
CAUTION - Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.
CAUTION - The use of optical instruments with this product will increase eye hazard.

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6. Diagnostic Software

6.1 Dealer mode

The purpose of the dealer mode is to prevent people taking out the CD inside the player at exhibitions, showrooms etc.. This mode disables the open/close function of the player.
The dealer mode can be switched on and off pressing keys [OPEN/CLOSE] and [STOP] of the CDR player simultaneously while switching on the unit. The dealer mode is stored in the flash memory and can only be changed by executing the above actions.

6.2 Dealer diagnostics

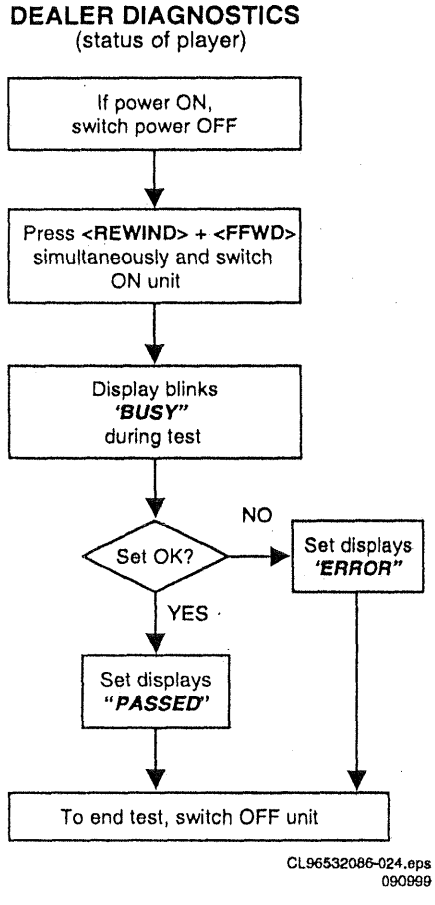

Figure 6-1

6.2.1 Description

The intention of the dealer diagnostics is to give an indication of the CDR player status. An inexperienced, even non-technical dealer will/can perform the test. Tests are executed automatically without need for external tools or disassembly of the unit. This test checks the CDR main board using the same tests as the electrical service diagnostics program. Only the result of the test, "PASSED" or "ERROR", will be shown on the display. Pressing keys [F FWD] and [REWIND] simultaneously while switching on the unit, starts the test. Switching off the unit ends the test.

6.2.2 Requirements to perform the test

- Working keyboard to start up the test.
- Working local display to check the output messages.

6.3 Electrical service diagnostics

ELECTRICAL SERVICE DIAGNOSTICS
(software versions, test for defective components)

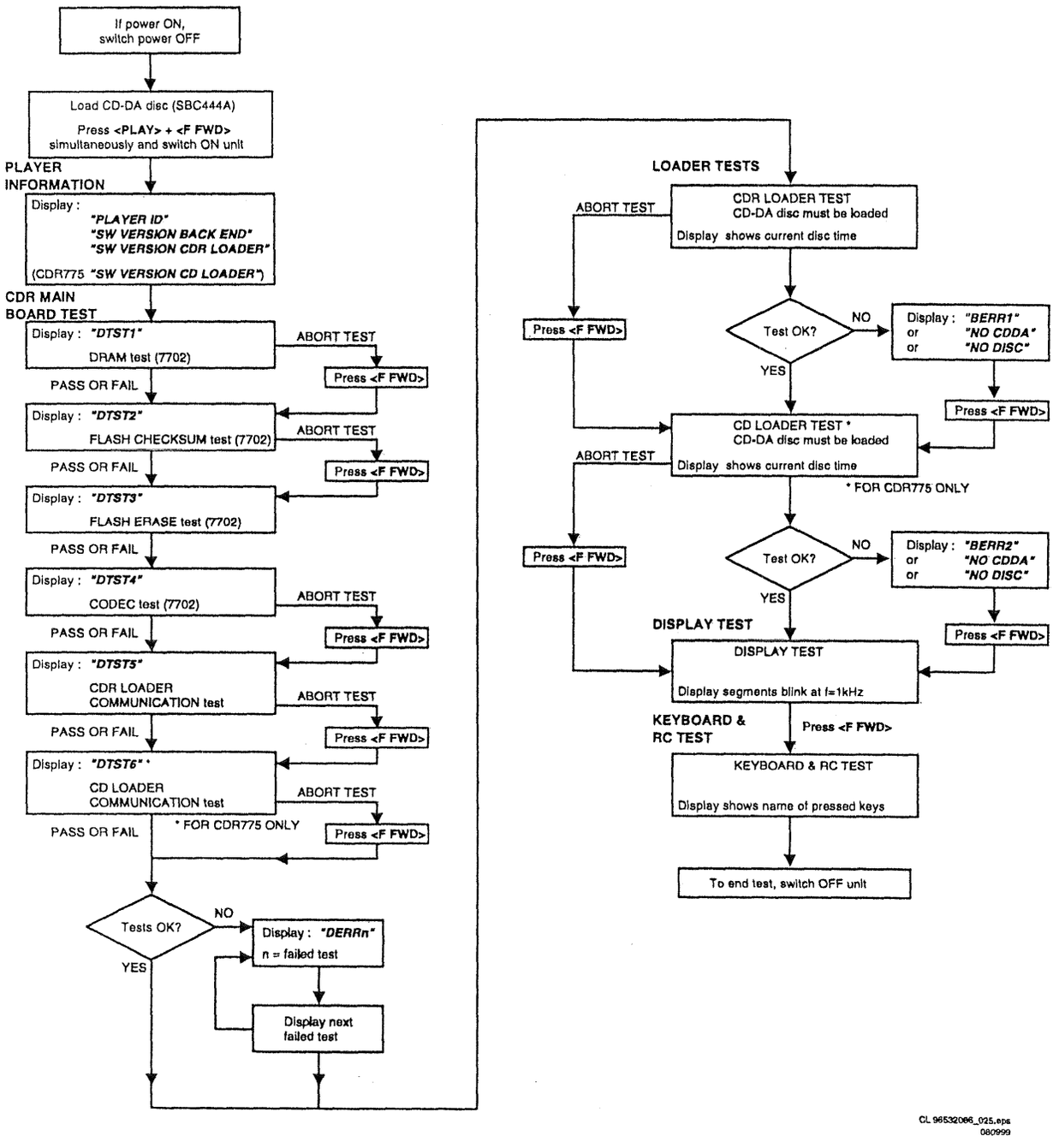

Figure 6-2

6.3.1 Description

The intention of the electrical service diagnostics is to show the software versions present in the player and to direct the dealer towards defective internal units. The units are : the CDR main board, the CDR loader, the CD loader in case of a CDR775 and the keyboard/display board. A sequence of tests is executed automatically. Some of the tests can be aborted or skipped without the result being taken into account. External tools or disassembly of the unit is not necessary to get the diagnostic information. Pressing keys [PLAY/PAUSE] and [F FWD] simultaneously while switching on the unit, starts the test. Switching off the unit ends the test.

6.3.2 Requirements to perform the test

- Working keyboard to start up the test.
- Working local display to check the output messages.
- A CD-DA disc with a minimum of 3 tracks in all trays to perform the disc test.

6.3.3 Description of the tests

Player information
In this part of the test the following important information can be checked without removing the cover :
- Recorder ID.
- SW-version back end of player.
- SW-version CDR loader.
- SW-version CD loader (only for CDR775).

CDR main board test
[F FWD] key. The message "DERRn" will be displayed with n indicating the faulty test number.
If one of the tests is aborted with the [F FWD] key, no error message will be displayed for this test. The flash data erase test ("DTST3") can not be aborted !
The CDR main board test consists out of :

DRAM test
Display : "DTST1". The DRAM used for buffer management is tested by writing, reading and verifying test patterns.

Flash checksum test
Display : "DTST2". This test checks the checksum of the player's SW stored in the flash.

Flash data erase
Display : "DTST3". During this test, all temporary information (CDtxt) in the flash is erased.

CODEC (ADC/DAC) test
Display : "DTST4". This test checks the CODEC IC by writing, reading and verifying test patterns. The test is not applicable for CDR950.

CDR communication test
Display : "DTST5". The communication between the host processor (DASP) and the CDR loader via the DSA-R-bus is tested.

CD communication test
Display : "DTST6"). The communication between the host processor (DASP) and the CD loader is tested. The test is only applicable for CDR775.

Loader tests
These tests determine if the CDR loader and the CD loader in case of a CDR775 work correctly. A CD-DA disc with a minimum of 3 tracks needs to be inserted in both loaders. A disc test is executed to check focus control, disc motor control, radial control and jump grooves control. The disc test is performed by audio play-back of 5 seconds at the beginning, middle and end of the disc.

CDR loader test
During the test, the current disc time is shown. In case of an error the message "BERR1" will be displayed and the [F FWD] key must be pressed to continue with the following test. Pressing the [F FWD] key also aborts this test.

CD loader test
For CDR775 only. During the test, the current disc time is shown. In case of an error the message "BERR2" will be displayed and the [F FWD] key must be pressed to continue with the following test. Pressing the [F FWD] key also aborts this test.

Display test
All segments will blink at a frequency of 1 Hz. Pressing the [F FWD] key will start the next test because the user has to check for himself if all segments work properly.

Keyboard and remote control tests
The test will give the user the ability to test every key without executing the function assigned to it. Therefore, the user needs to press every key on the keyboard and the remote control. The display will show the name of the key being pressed. Pressing more than one key at once will give an unpredictable result except for the service combinations : [PLAY/PAUSE] + [STOP], [PLAY/PAUSE] + [F FWD], [F FWD] + [REWIND], [ERASE] + [RECORD], [PLAY/PAUSE] + [RECORD], [OPEN/CLOSE] + [PROGRAM].

6.4 Mechanical service diagnostics

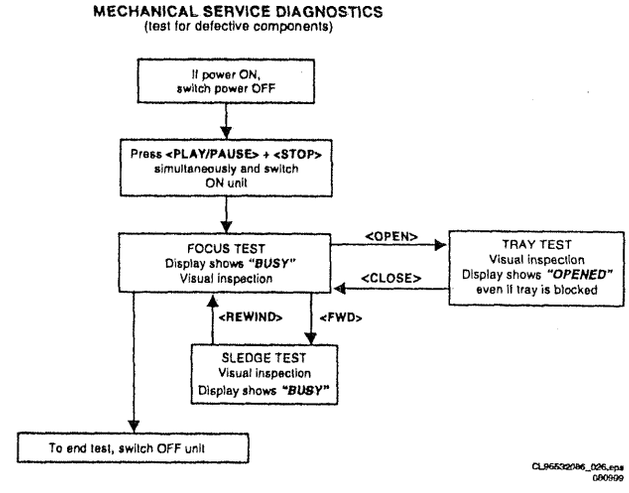

Figure 6-3

6.4.1 Description

No external tools are required to perform this test. The cover needs to be removed because the user has to check the movements of the tray, focus and sledge visually. Pressing keys [PLAY/PAUSE] and [STOP] simultaneously while switching on the unit, starts the test. Switching off the unit ends the test. In case of a CDR775, one can check the CD loader mechanics in the same way by pressing the above key combination on the CD player keys.

6.4.2 Requirements to perform the test

- Working keyboard to cycle through the tests and to start up the test.
- Working local display to check the output messages.

6.4.3 Description of the tests

Focus control test
The focussing lens is continuously moving up and down. The display reads "BUSY".

Sledge control test
After pressing [F FWD] the sledge continuously moves up and down. Pressing [REWIND] stops the sledge at the position it is in and the focus control test resumes. The display reads "BUSY".

Tray control test
This test starts from within the focus control test routine. Pressing [OPEN/CLOSE] moves the tray in or out. In the tray open position one can initiate focus and sledge tests by pressing [F FWD]. One has to stop these tests pressing [REWIND] before it is possible to close the tray again. Depending on the action the display reads "OPEN", "OPENED", "CLOSE" or "BUSY".

6.5 DC-erase service mode

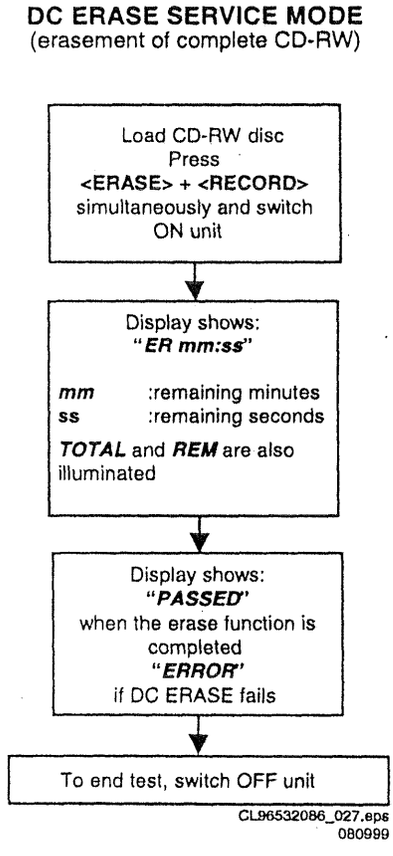

Figure 6-4

6.5.1 Description

This test is initiated by pressing [ERASE] and [RECORD] simultaneously while switching on the unit. The player will erase a complete CD-RW disc (including PMA and ATIP lead out area) at speed N=2. The display shows the countdown of the remaining time required for the operation to complete. The format is "ER mm:ss", where "mm" are the remaining minutes and "ss" the remaining seconds. After completion the message "PASSED" is shown, and the player has to be switched off and on again to start up in normal operating mode. Switching off the unit before completion of the test, leaves the disc in an unpredictable state. In such case only a complete DC-erase procedure can recover the CD-RW disc.

6.5.2 Requirements to perform the test

- Functional CDR player.
- A CD-RW audio disc must be present in the tray.

7. Faultfinding trees

7.1 CDR-Module

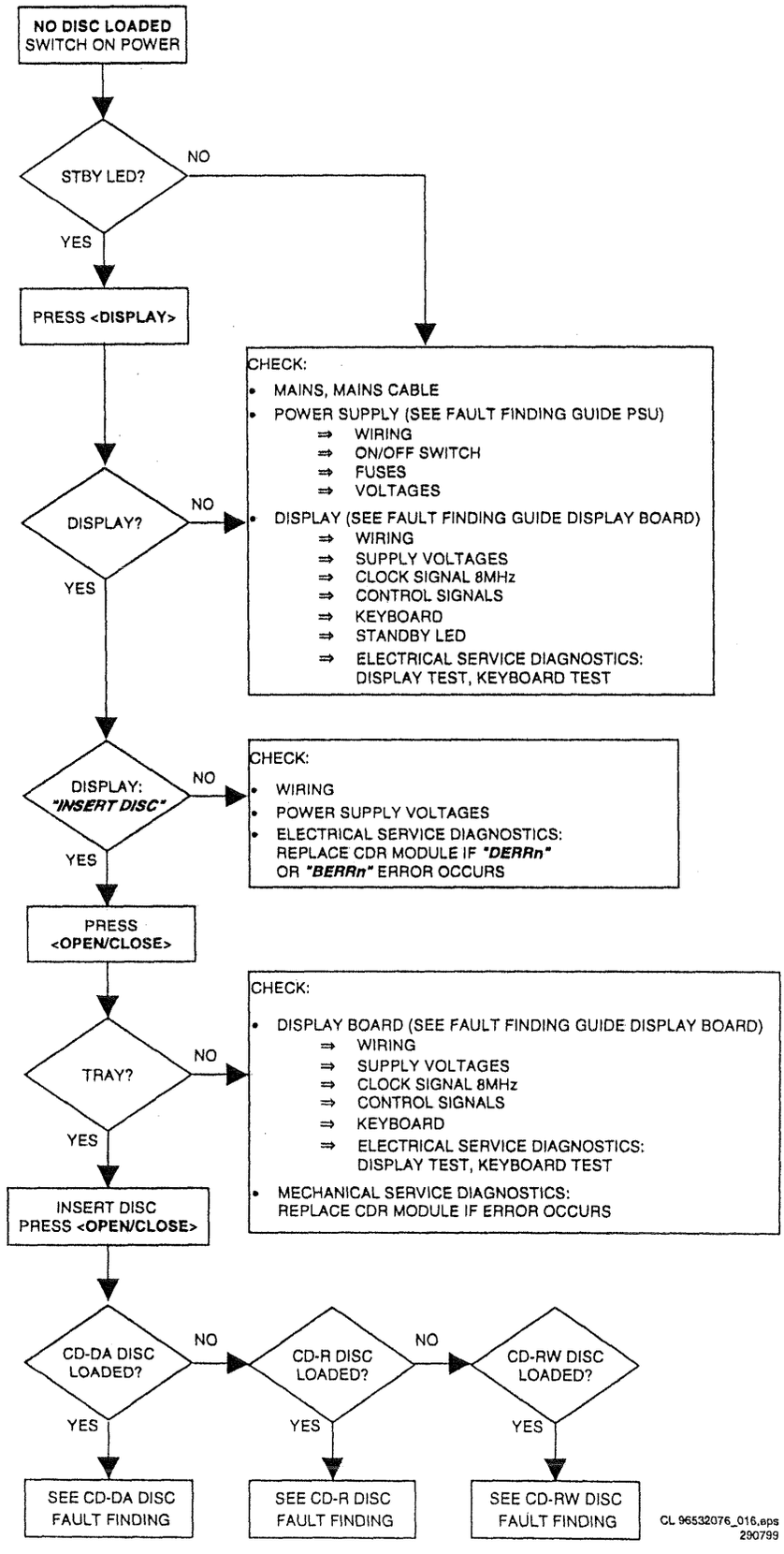

Figure 7-1

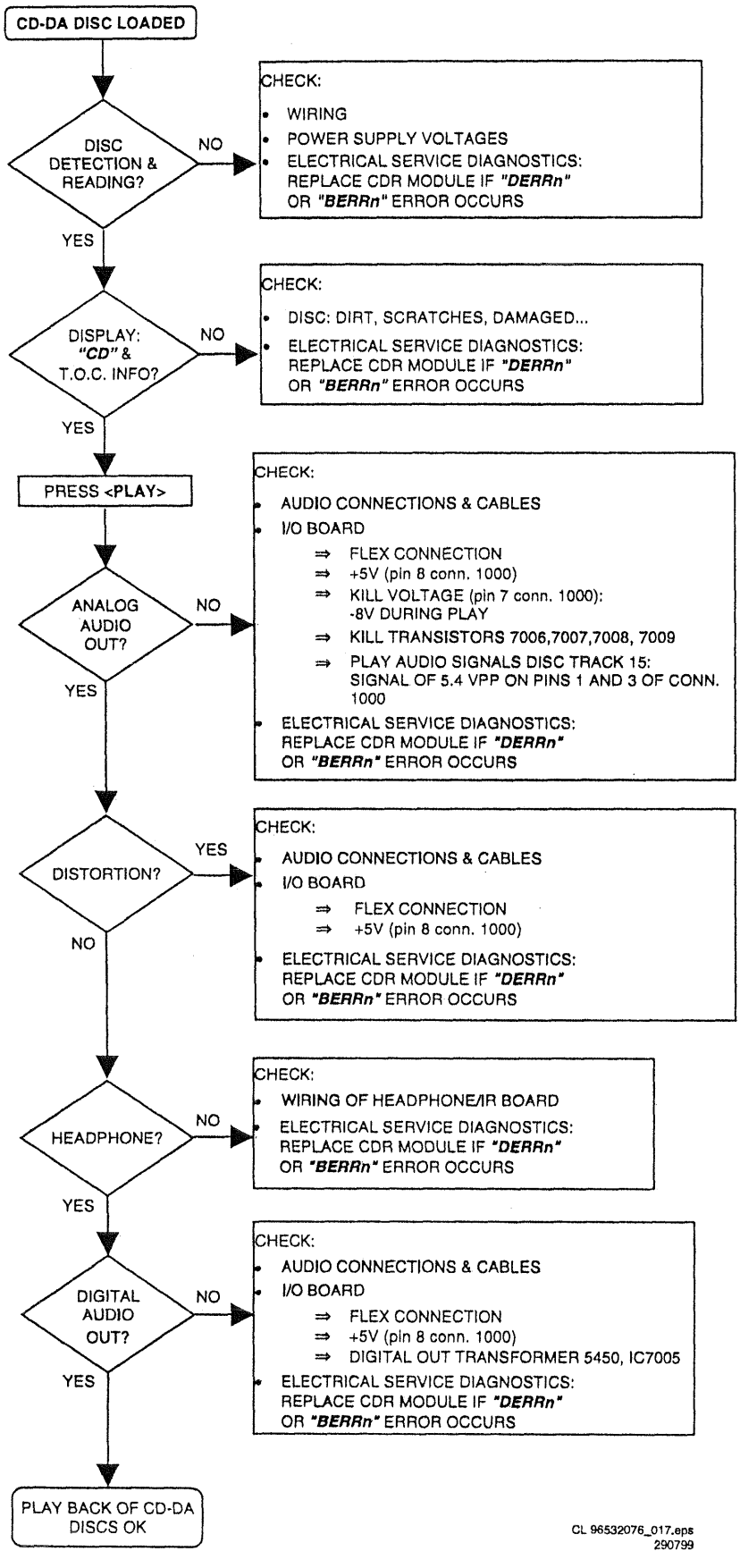
CD-DA DISC LOADED
DISC DETECTION & READING?
NO
CHECK:
• WIRING
• POWER SUPPLY VOLTAGES
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
DISPLAY: "CD" & T.O.C. INFO?
NO
CHECK:
• DISC: DIRT, SCRATCHES, DAMAGED...
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
PRESS <PLAY>
ANALOG AUDIO OUT?
NO
CHECK:
• AUDIO CONNECTIONS & CABLES
• I/O BOARD
⇒ FLEX CONNECTION
⇒ +5V (pin 8 conn. 1000)
⇒ KILL VOLTAGE (pin 7 conn. 1000): -8V DURING PLAY
⇒ KILL TRANSISTORS 7006,7007,7008, 7009
⇒ PLAY AUDIO SIGNALS DISC TRACK 15: SIGNAL OF 5.4 VPP ON PINS 1 AND 3 OF CONN. 1000
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
DISTORTION?
YES
CHECK:
• AUDIO CONNECTIONS & CABLES
• I/O BOARD
⇒ FLEX CONNECTION
⇒ +5V (pin 8 conn. 1000)
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
NO
HEADPHONE?
NO
CHECK:
• WIRING OF HEADPHONE/IR BOARD
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
DIGITAL AUDIO OUT?
NO
CHECK:
• AUDIO CONNECTIONS & CABLES
• I/O BOARD
⇒ FLEX CONNECTION
⇒ +5V (pin 8 conn. 1000)
⇒ DIGITAL OUT TRANSFORMER 5450, IC7005
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
PLAY BACK OF CD-DA DISCS OK
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Figure 7-2

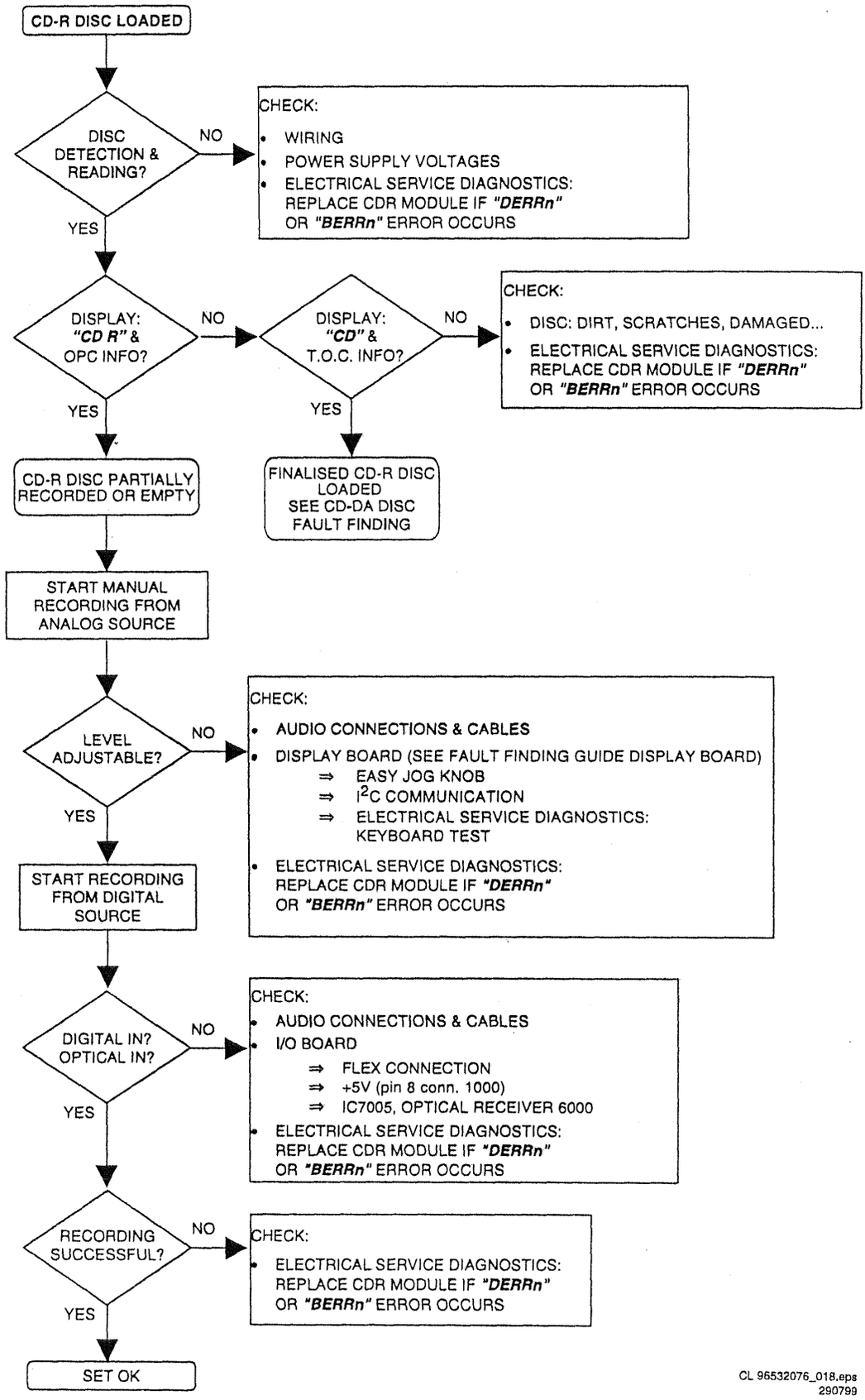
CD-R DISC LOADED
DISC DETECTION & READING?
NO
CHECK:
• WIRING
• POWER SUPPLY VOLTAGES
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
DISPLAY: "CD R" & OPC INFO?
NO
DISPLAY: "CD" & T.O.C. INFO?
NO
CHECK:
• DISC: DIRT, SCRATCHES, DAMAGED...
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
YES
CD-R DISC PARTIALLY RECORDED OR EMPTY
FINALISED CD-R DISC LOADED SEE CD-DA DISC FAULT FINDING
START MANUAL RECORDING FROM ANALOG SOURCE
LEVEL ADJUSTABLE?
NO
CHECK:
• AUDIO CONNECTIONS & CABLES
• DISPLAY BOARD (SEE FAULT FINDING GUIDE DISPLAY BOARD)
⇒ EASY JOG KNOB
⇒ I2C COMMUNICATION
⇒ ELECTRICAL SERVICE DIAGNOSTICS: KEYBOARD TEST
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
START RECORDING FROM DIGITAL SOURCE
DIGITAL IN? OPTICAL IN?
NO
CHECK:
• AUDIO CONNECTIONS & CABLES
• I/O BOARD
⇒ FLEX CONNECTION
⇒ +5V (pin 8 conn. 1000)
⇒ IC7005, OPTICAL RECEIVER 6000
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
RECORDING SUCCESSFUL?
NO
CHECK:
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
SET OK
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Figure 7-3

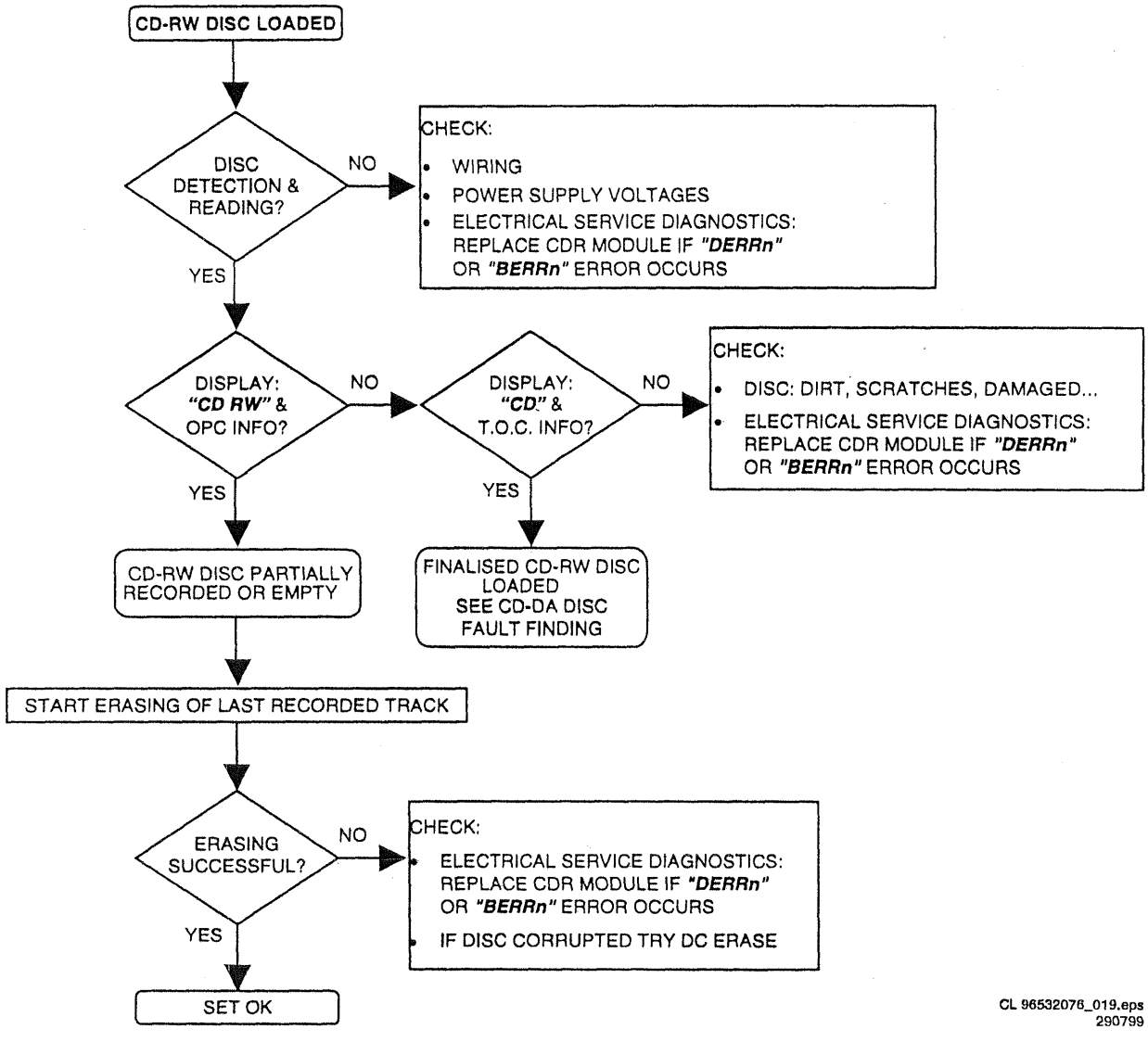
CD-RW DISC LOADED
DISC DETECTION & READING?
NO
CHECK:
• WIRING
• POWER SUPPLY VOLTAGES
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
DISPLAY: "CD RW" & OPC INFO?
NO
DISPLAY: "CD" & T.O.C. INFO?
NO
CHECK:
• DISC: DIRT, SCRATCHES, DAMAGED...
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
YES
YES
CD-RW DISC PARTIALLY RECORDED OR EMPTY
FINALISED CD-RW DISC LOADED SEE CD-DA DISC FAULT FINDING
START ERASING OF LAST RECORDED TRACK
ERASING SUCCESSFUL?
NO
CHECK:
• ELECTRICAL SERVICE DIAGNOSTICS: REPLACE CDR MODULE IF "DERRn" OR "BERRn" ERROR OCCURS
• IF DISC CORRUPTED TRY DC ERASE
YES
SET OK
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Figure 7-4

7.2 CD Module

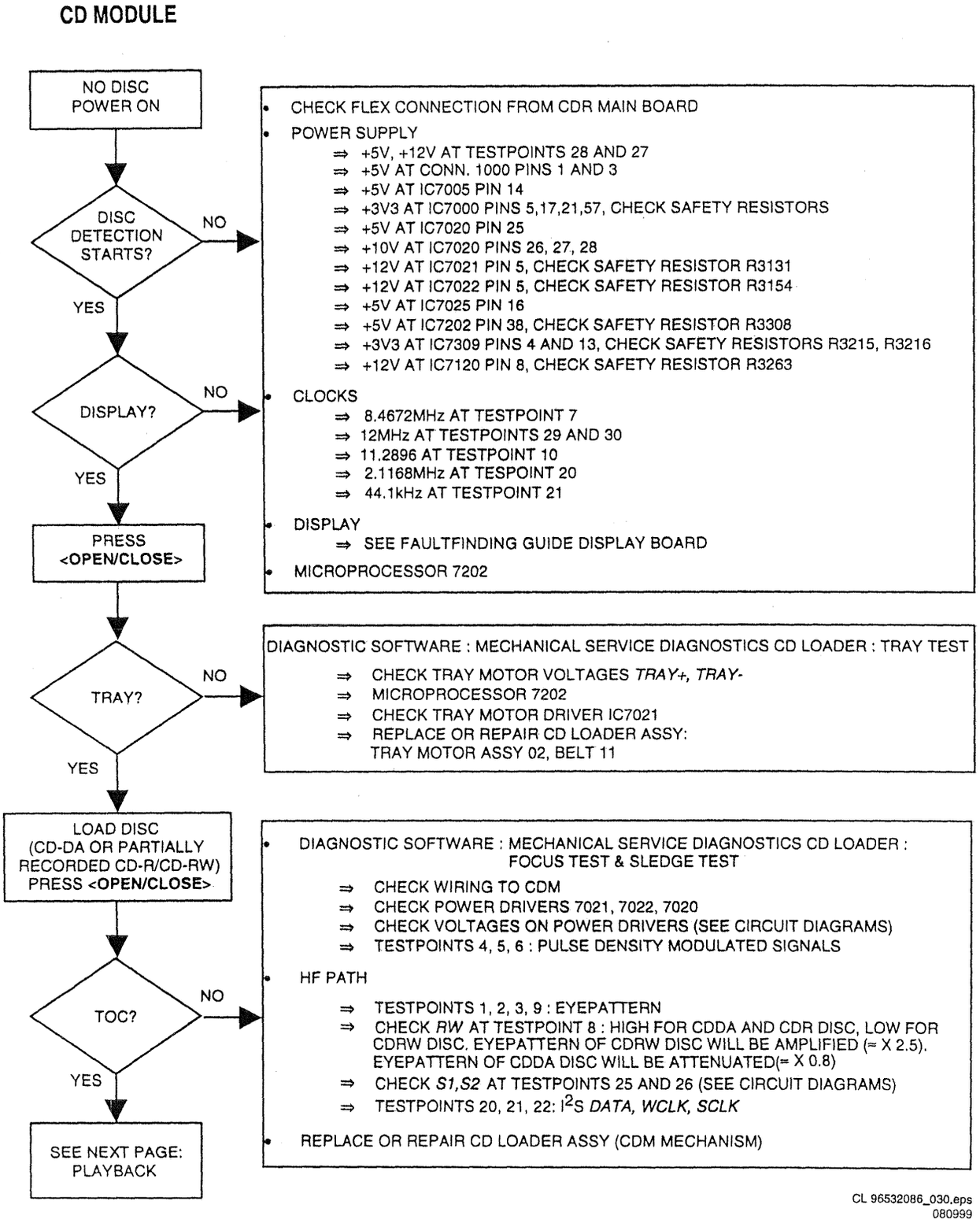

Figure 7-5

CD MODULE PLAYBACK

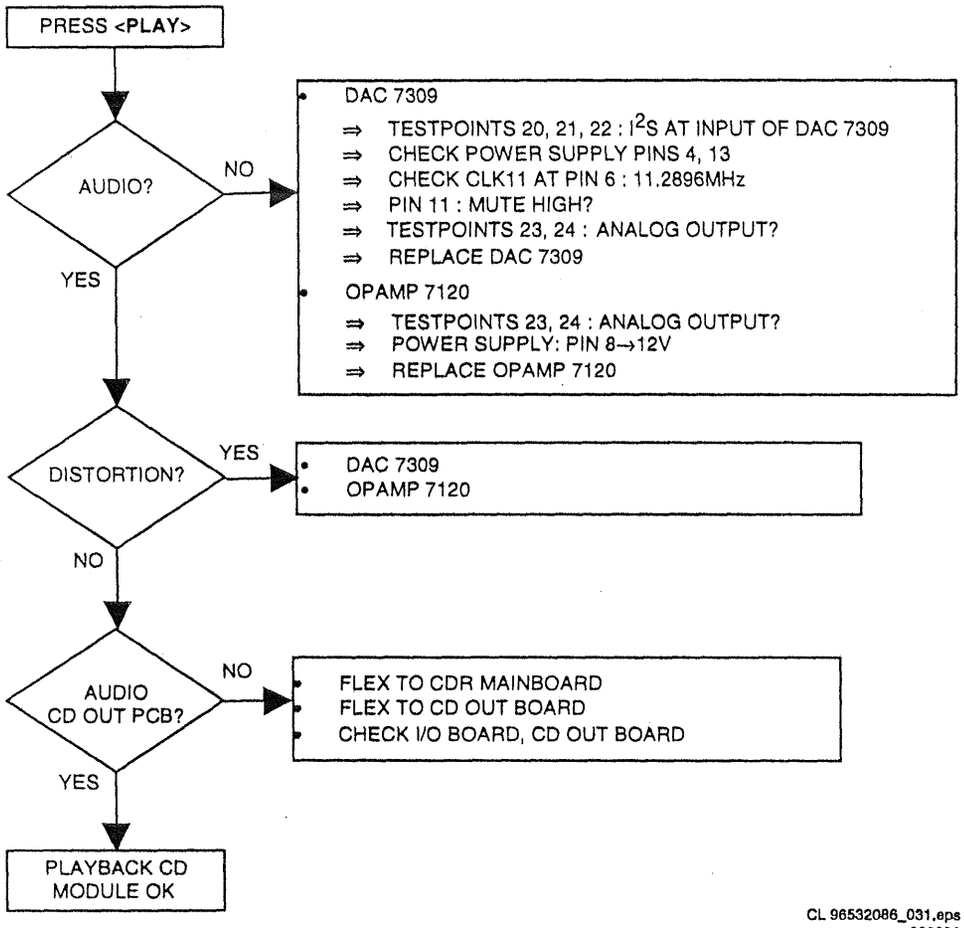

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Figure 7-6

8. Faultfinding Guide

8.1 Display Board

8.1.1 Description of display board

General description

The display board has three major parts : the FTD (Fluorescent Tube Display), the display controller TMP87C874F and the keyboard. The display controller is controlled by the DASP master processor on the CDR main board. The communication protocol used is I2C. So all the information between DASP and display controller goes via the SDA or I2C DATA and SCL or I2C CLK lines. Communication is always initiated by the DASP on the CDR main board. Unlike the previous generations of CDR players, the interrupt generated by the display controller at key-press or reception of remote control is not used. Instead, the DASP polls the display controller for these events.

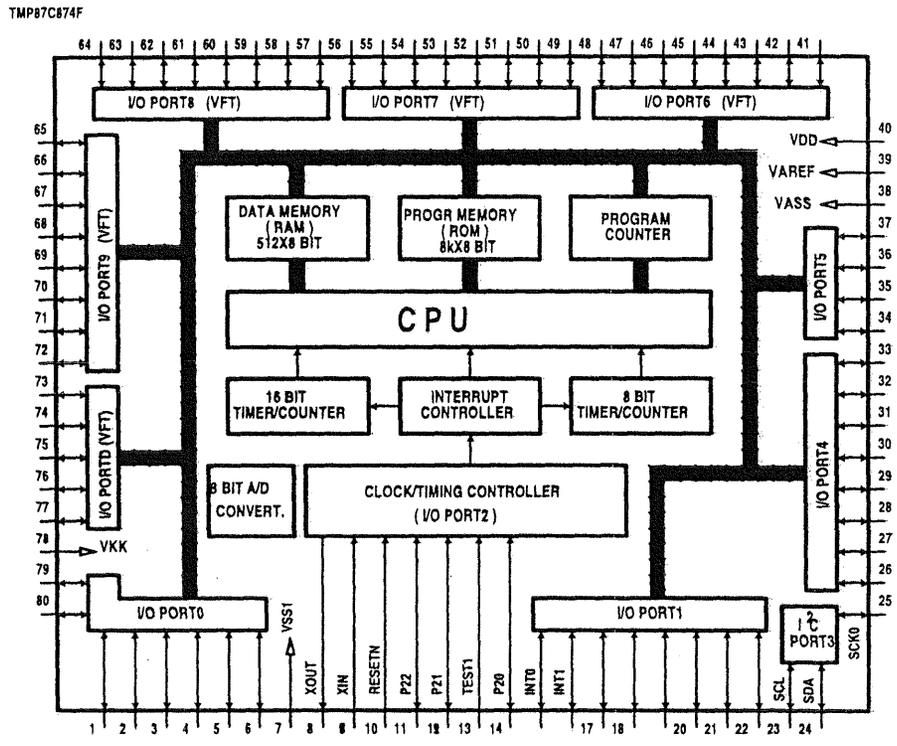
Display controller TMP87C874F

TMP87C874F (IC7104) is a high speed and high performance 8-bit single chip microprocessor, containing 8-bit A/D conversion inputs and a VFT (Vacuum Fluorescent Tube) driver. In this application, its functions are :

- slave microprocessor.
- FTD driver.
- generates the square wave for the filament voltage required for an AC FTD.
- generates the grid and segment scanning for the FTD.
- generates the scanning grid for the key matrix.
- input for remote control.

All the communication runs via the serial bus interface I2C. The display controller uses an 8MHz resonator as clock driver.

BLOCK DIAGRAM



PIN DESCRIPTIONS

INT0	external interrupt input 0
INT1	external interrupt input 1
RESETN	reset signal input, active low
SCL	I2C-bus serial clock input/output
SDA	I2C-bus serial data input/output
TEST	test pin, tied to low
VAREF	analog reference voltage input
VASS	analog reference ground
VDD	+5V
VKK	VFT driver power supply
VSS	ground
XIN, XOUT	resonator connecting pins for high-frequency clock

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Figure 8-1

8.1.2 Test instructions

Supply voltages

The display board receives several voltages via connector 1119 (and connector 1121 for CDR570/930).

- VFTD : -38V ±5% measured at pin 2 of conn. 1119.
- VDC1-VDC2 : 3V8 ±10% measured between pin 1 and 3 of conn. 1119.
- +5V : +5V ±5% measured at pin 10 of conn. 1119 (pin 4 of conn. 1121 for CDR770).

Voltages VFTD, VDC1 and VDC2 are produced in the power supply unit and sent to the display board via the CDR main board. The +5V voltage is produced on the CDR main board as D5V.

Clock signal

As clock driver for the display controller, a resonator of 8 MHz (1110) is used. The signal can be measured at pins 8 and 9 of the display controller : 8 MHz ±5%.

Control signals

RESET

The reset signal comes via pin 4 of conn. 1119 from the DASP master processor on the CDR main board (SYS_RESET). The reset is low active. It should be kept low during power up for at least 3 machine cycles with supply voltage in operating range and a stable clock signal (1 machine cycle = 12 x 1/Fc (8 MHz) sec.). During normal operation, the reset should be high (3V3). The high signal is 3V3 because the DASP operates on 3V3.

I2C DATA/I2C CLK

These lines connect to the DASP master processor via respectively pin 5 and pin 7 of conn. 1119 (pin 5 of conn. 1119 and pin 1 of conn. 1121 for CDR570/930). When there is no communication, they should have the high level (+5V). The oscillogram below gives an indication of how these signals should look like.

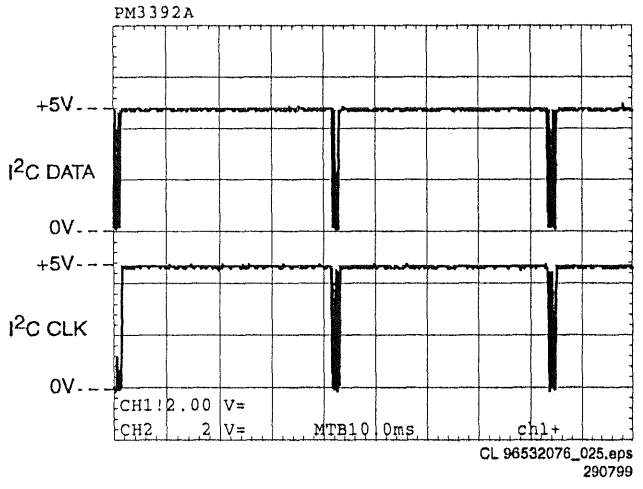

Figure 8-2 'I2C signals'

FTD drive lines

Filament voltage

Should measure 3.8V ±10% (=VDC1-VDC2) between pins 1-2-3 and pins 45-46-47 (pins 1-2 and pins 48-49 for CDR770) of the FTD (1113).

Grid lines

Level and timing of all grid lines, G1-->G15, can be checked either at the FTD itself or at the display controller. Grid lines G13, G14 and G15 each have an extra current amplifier in line : T7203 for G13, T7204 for G14 and T7100 for G15. A typical grid line signal shows in the oscillogram below.

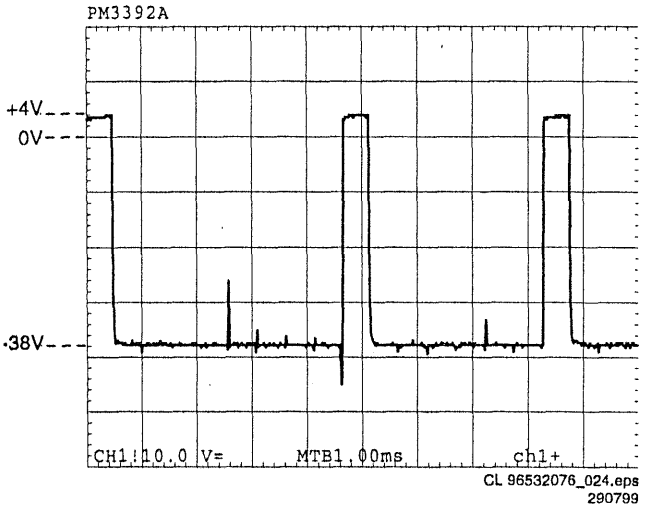

Figure 8-3 'Gridline'

Segment lines

Level and timing of all segment lines, P1-->P21 (P1-->P20 for CDR770), can be checked either at the FTD itself or at the display controller. The data on these segment lines however, depends on the characters displayed. The oscillogram below shows a segment line with data. A segment line without data maintains a -38V level.

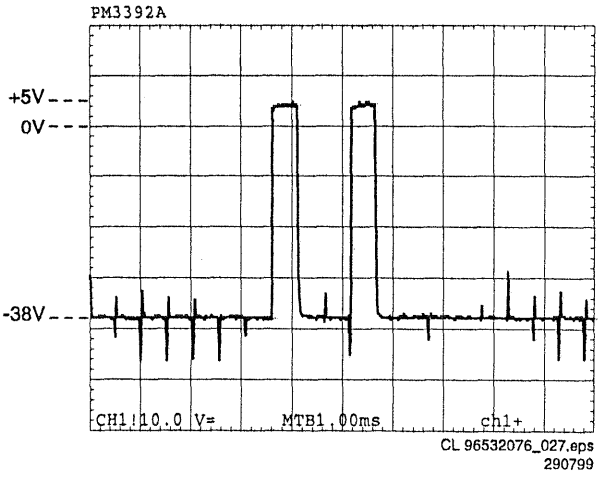

Figure 8-4 'Segment line'

Key matrix lines

The lines connected to pins 34, 35, 36 and 37 of the display controller act as matrix scanners. Without a key pressed, they maintain a low level. As soon as a key is pressed, the scanning line connected to that key puts out a scanning signal, which should look like the oscillogram below. This scanning signal goes via the pressed key to I/O port 4 of the display controller (pins 28 to 33). The display controller can now determine which key has been pressed. Without a key pressed, pins 28 to 33 of the display controller maintain a high level (+5V).

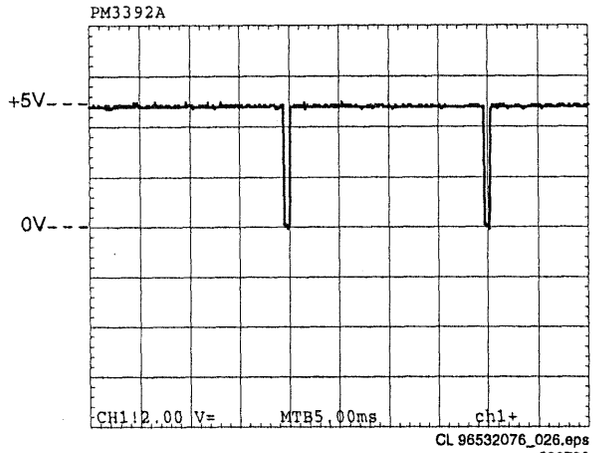

Figure 8-5 'Key matrix scan line'

Easy jog knob

Rotary operation
The easy jog knob (1050) incorporates a whole heap of user control possibilities in just one knob. Without the knob being operated, pin 1 and 3 of the knob (and thus pin 16 and 17 of the display controller), maintain the +5V level. Turning the knob clockwise briefly connects pin 1 to GND followed by pin 3.

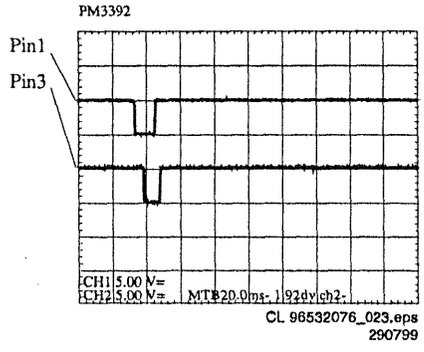

Figure 8-6 'Turn clockwise'

Turning the knob anti-clockwise briefly connects pin 3 to GND followed by pin 1.

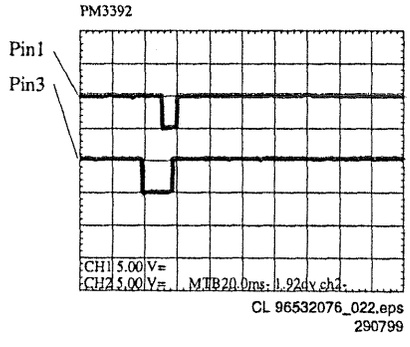

Figure 8-7 'Turn anti-clockwise'

The pulses created this way arrive at pin 16 and 17 of the display controller. The first pulse to arrive tells the controller the direction of the rotation. Counting the pulses reveals the amount of rotation. Combining and decoding this information, the display controller will execute the appropriate task.

Push button operation
This button connects to the key matrix lines and thus the operation is identical to the ordinary keys. Without being pressed, pin 4 of the easy jog maintains the low level, pin 5 the high level. When pressed the scanning signal goes through the closed contact of pins 4 and 5, and can be checked at both pins.

IR receiver - remote control
In the CDR570/930 the IR receiver TSOP1736 (6101) is mounted on the display board. In the CDR770 that same IR receiver (6200) is mounted on a small board together with the headphone socket. In the CDR775 the IR receiver (6200) is mounted on its own small board. In all versions the IR receiver connects to the display controller. The signal coming from the receiver can be checked at pin 22 of the display controller. This signal is normally high (+5V). When the remote control is being operated, pulses mixed in with the +5V can be measured. The oscillogram gives an indication of how the signal looks like with the RC being operated.

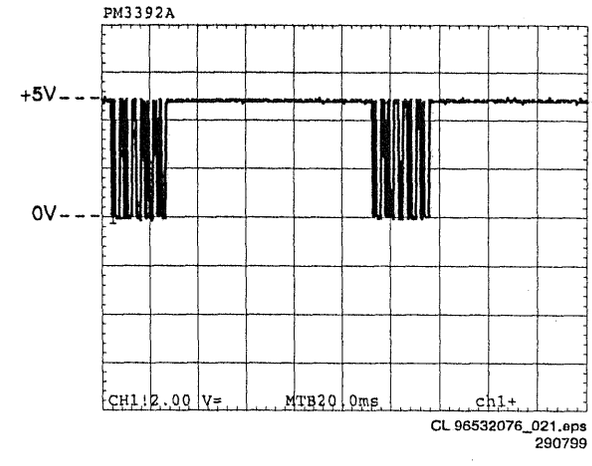

Figure 8-8 'IR receiver signal'

8.1.3 Display board troubleshooting guide

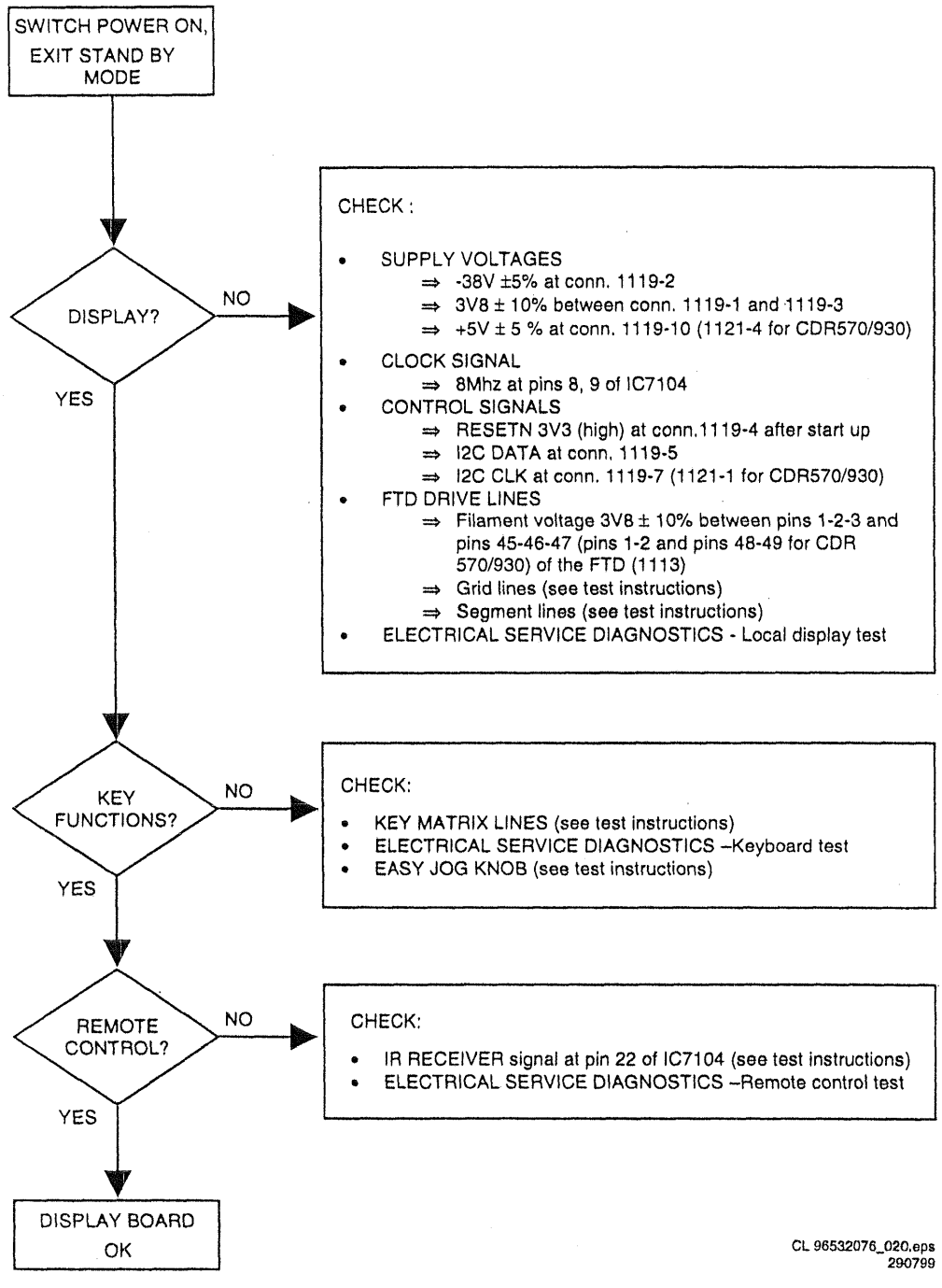

Figure 8-9 'Display board troubleshooting'

8.2 Power Supply Unit 20PS317

8.2.1 Description of PSU 20PS317

MOSFET 7125 is used as a power switch controlled by the controller IC7110. When the switch is closed, energy is transferred from mains to the transformer. This energy is supplied to the load when the switch is opened. Through control of the switch-on time, the energy transferred in each cycle is regulated so that the output voltages are independent of load or input voltage variations. The controlling device MC44603 is an integrated pulse width modulator. A clock signal initiates power pulses at a fixed frequency. The termination of each output pulse occurs when a feedback signal of the inductor current reaches a threshold set by the error signal. In this way the error signal actually controls the peak inductor current on cycle-by-cycle basis.

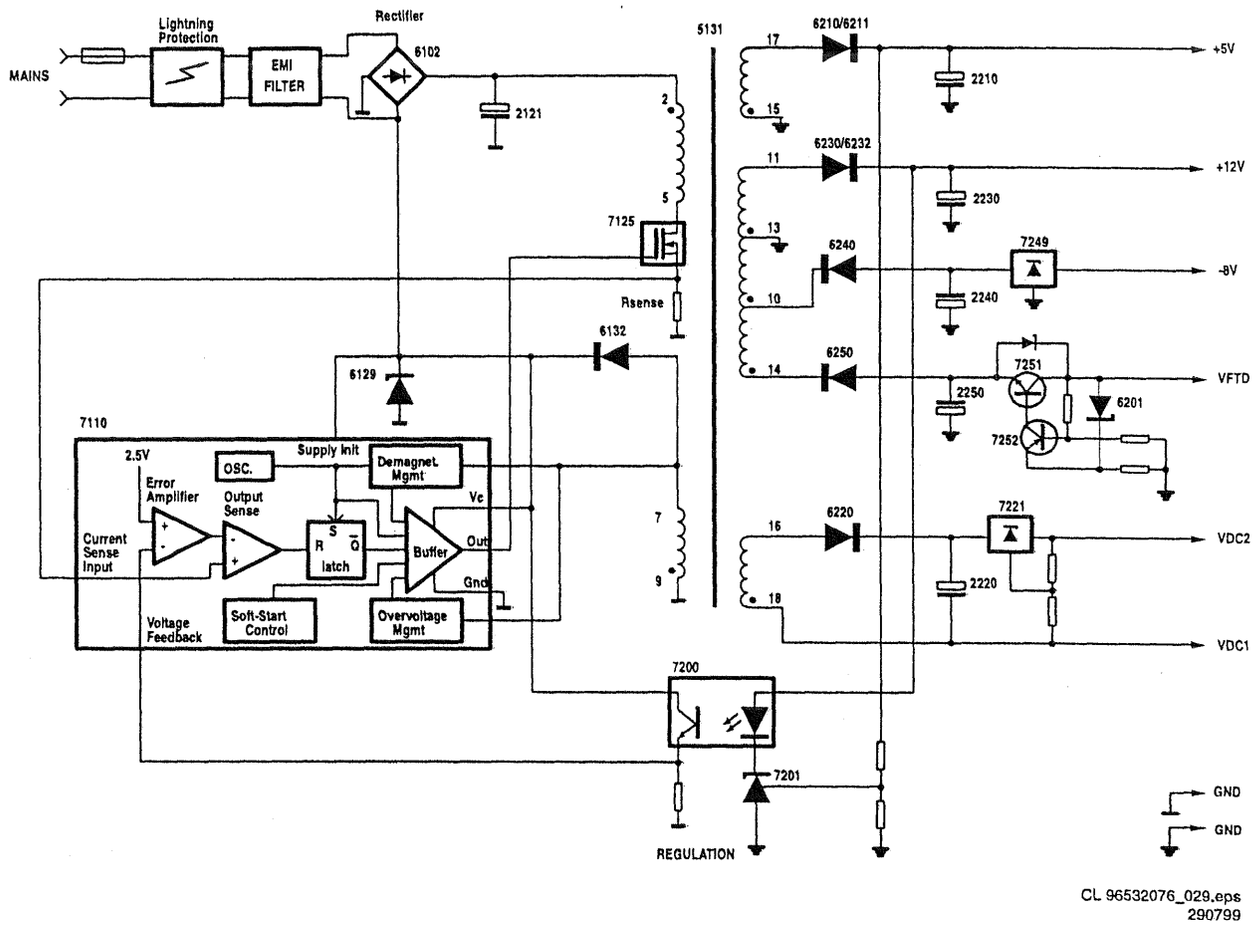

Figure 8-10 'Blockdiagram PSU 20PS317'

Description of controller MC44603

The MC44603 is an enhanced high performance controller that is specifically designed for off-line and DC-to-DC converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded or shorted. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters. It is optimised to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

Pin connections

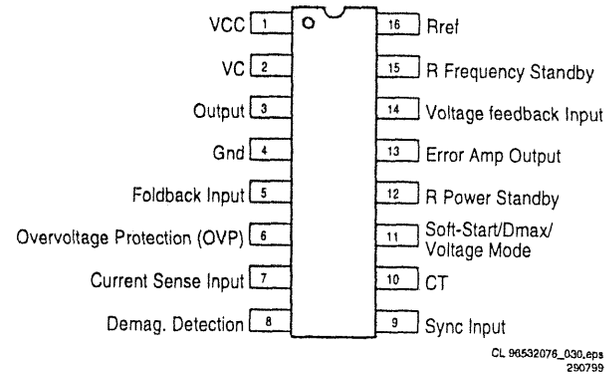

Figure 8-11

Pin function description

Pin	Name	Description
1	VCC	This pin is the positive supply of the IC. The operating voltage range after start-up is 9.0 to 14.5 V.
2	VC	The output high state (VOH) is set by the voltage applied to this pin.
3	Output	Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or bipolar transistors.
4	Gnd	The groundpin is a single return, typically connected back to the power source.
5	Foldback Input	The foldback function provides overload protection.
6	Overvoltage Protection	When the overvoltage protection pin receives a voltage greater than 2.5V, the device is disabled and requires a complete restart sequence.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input.
8	Demagnetisation Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetisation pin an indication of the magnetisation state of the flyback transformer. A zero voltage detection corresponds to complete core saturation.
9	Synchronisation Input	The synchronisation input pin can be activated with either a negative pulse going from a level between 0.7V and 3.7V to Gnd or a positive pulse going from a level between 0.7V and 3.7V up to a level higher than 3.7V. The oscillator runs free when Pin 9 is connected to Gnd.
10	C_T	The normal mode oscillator frequency is programmed by the capacitor CT choice together with the Rref resistance value. CT, connected between Pin 10 and Gnd, generates the oscillator sawtooth.
11	Soft-Start/Dmax/Voltage-Mode	A capacitor, resistor or a voltage source connected to this pin limits the switching duty-cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603 can be shut down.
12	RP Standby	A voltage level applied to the RP Standby pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation (i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop.
15	RF Standby	The reduced frequency or standby frequency programming is made by the RF Standby resistance choice.
16	Rref	Rref sets the internal reference current. The internal reference current ranges from 100µA to 500µA. This requires that 5.0kΩ ≤ Rref ≤ 25kΩ.

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Figure 8-12

Block diagram of MC44603

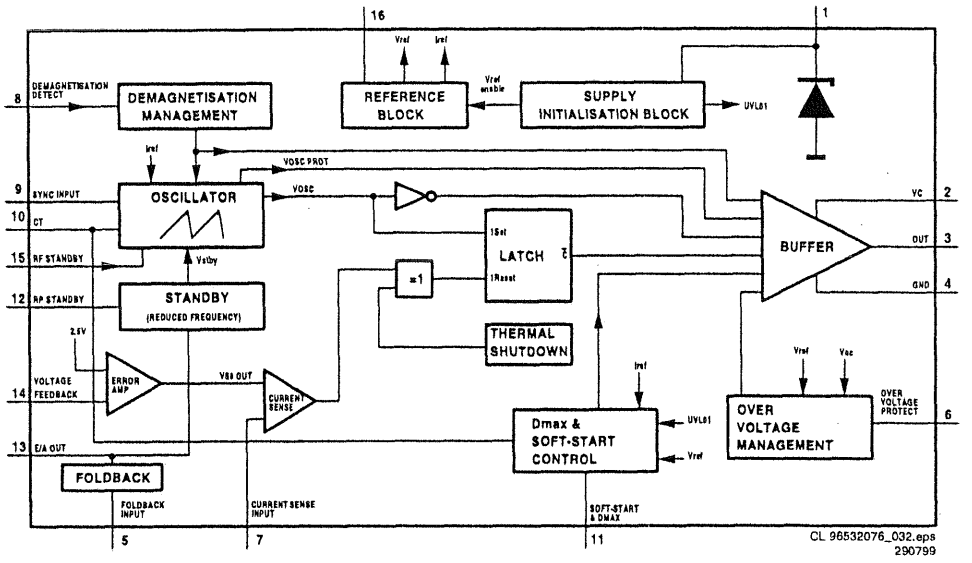


Figure 8-13

Operating description of MC44603

The input voltage Vcc (pin 1) is monitored by a comparator with hysteresis, enabling the circuit at 14.5V and disabling the circuit below 7.5V. The error amplifier compares a voltage Vfb (pin 14) related to the output voltage of the power supply, with an internal 2.5V reference. The current sense comparator compares the output of the error amplifier with the switch current Isense (pin 7) of the power supply. The output of the current sense comparator resets a latch, which is set every cycle by the oscillator. The output stage is a totem pole, capable of driving a MOSFET directly.

Start up sequence of PSU 20PS317

t1: Charging the capacitors at Vcc
C2129 will be charged via R3123 and R3134, C2133 and C2111 via R3129. The output is switched off during t1.
t2: Charging of output capacitors
When the input voltage of the IC exceeds 14.5V, the circuit is enabled and starts to produce output pulses. The current consumption of the circuit increases to about 17mA, depending on the external loads of the IC. At first, the capacitors at the Vcc pin will discharge because the primary auxiliary voltage, coming from winding 7-9 is below the Vcc voltage. At some moment during t2, the primary auxiliary voltage reaches the same level as Vcc. This primary auxiliary voltage now determines the Vcc voltage.
t3: Regulation
The output voltage of the power supply is in regulation.
t4: Overload
When the output is shorted, the supply voltage of the circuit will decrease and after some time drop below the lower threshold voltage. At that moment, the output will be disabled and the process of charging the Vcc capacitors starts again. If the output is still shorted at the next t2 phase, the complete start- and stop sequence will repeat. The power supply goes in a hiccup mode.

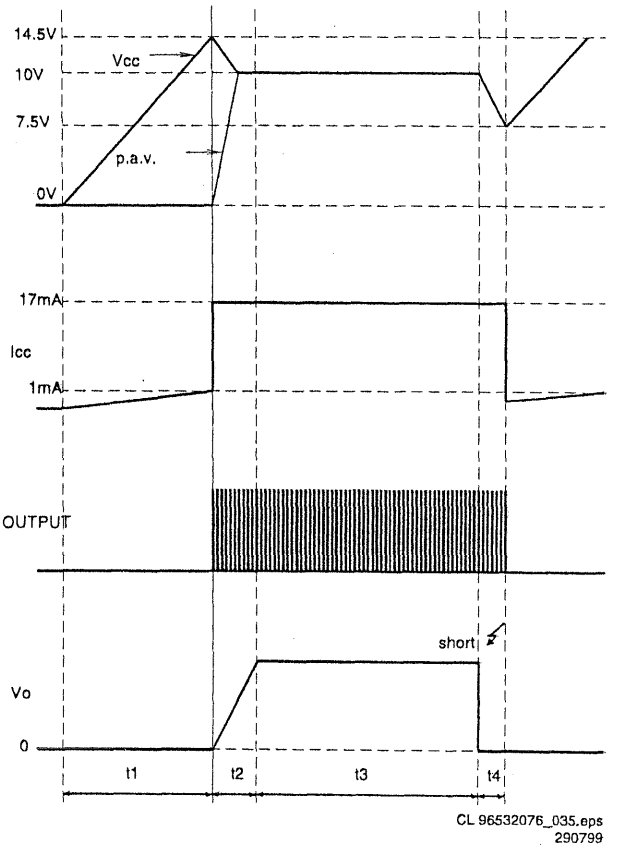


Figure 8-14 'Start-up sequence'

Regulation of PSU 20PS317

Figure 8-14 shows the most relevant signals during the regulation phase of the power supply.
The oscillator voltage ramps up and down between V1 and V2. The voltage at the current sense terminal is compared every cycle with the output of the error amplifier Vcomp. The output

is switched off when the current sense level exceeds the level at the output of the error amplifier.
TimeON phase : A drain current will flow from the positive supply at pin 2 of the transformer through the transformer's primary winding, the MOSFET and Rsense to ground. As the positive voltage at pin 2 of the transformer is constant, the current will increase linearly and create a ramp dependent on the mains voltage and the inductance of the primary winding. A certain amount of energy is stored in the transformer in the form of a magnetic field. The polarity of the voltages at the secondary windings is opposite to the primary winding so that the diodes are non-conducting in this phase.
TimeDIODE phase : When the MOSFET is switched off, energy is no longer supplied to the transformer. The inductance of the tranformer now tries to maintain the current which has been flowing through it at a constant level. The polarity of the voltage from the transformer therefore reverses. This results in a current flow through the transformer's secondary winding via the now conducting diodes, electrolytic capacitors and the load. This current is also ramp shaped but decreasing.
TimeDEAD phase : when the stored energy has been supplied to the load, the current in the secondary windings stops flowing. At this point, the drain voltage of the MOSFET will drop to the voltage of C2121 with a ringing caused by the drain-source capacitance with the primary inductance.
The oscillator will start a next cycle which consists of the above described three phases. The time of the different phases depends on the mains voltage and the load.
TimeDEAD is maximum with an input of 400VDC and a minimum load. It will be zero with an input of 100VDC and an overload.

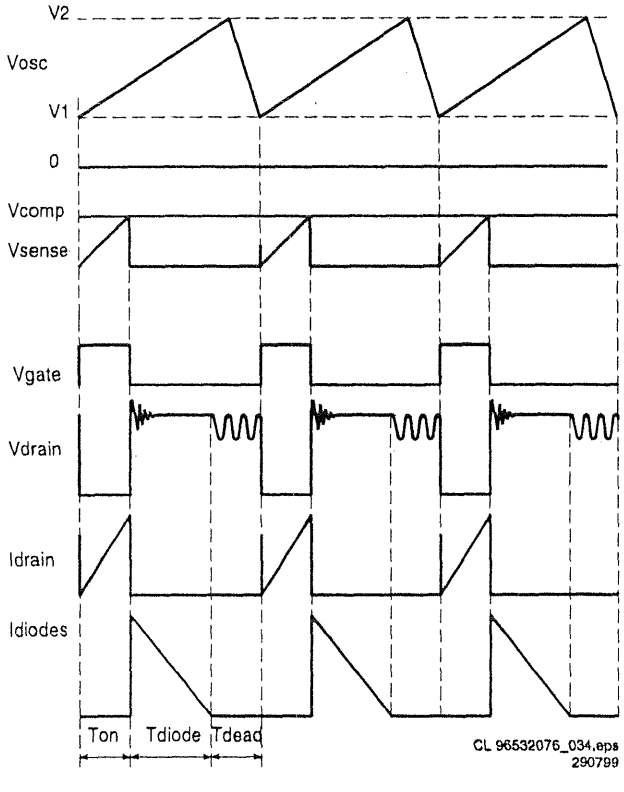
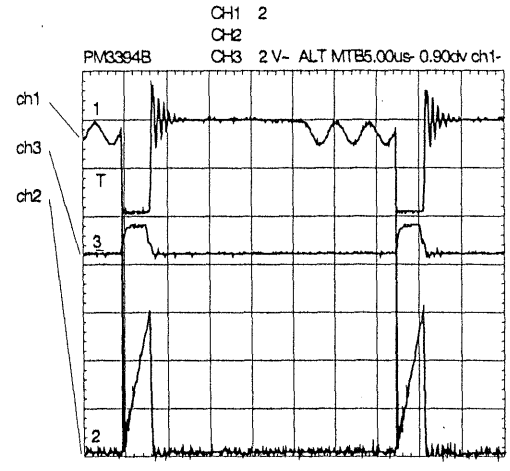
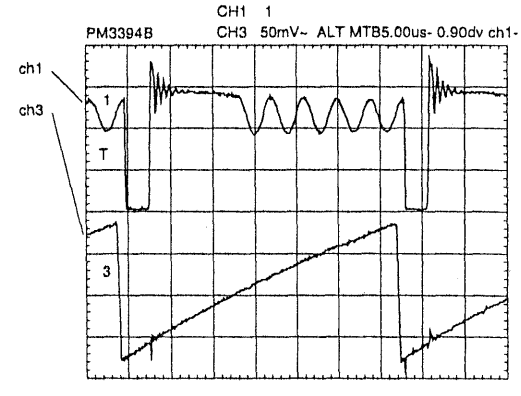


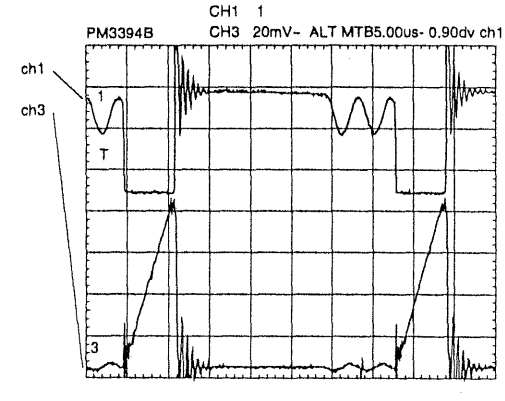
Figure 8-15 'Regulation'



ch1 : Drain voltage
ch2 : Drain current
ch3 : Gate voltage



ch1 : Drain voltage
ch2 : Oscillator voltage



ch1 : Drain voltage
ch3 : Sense voltage

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Figure 8-16 'Oscillograms'

Circuit description of PSU 20PS317

Input circuit
The input circuit consists of a lightning protection circuit and an EMI filter.
The lightning protection comprises R3120, gasarrestor 1125 and R3124. The EMI filter is formed by C2120, L5120, C2125 and C2126. It prevents inflow of noise into the mains.

Primary rectifier/smoothing
The AC input is rectified by rectifier bridge 6102 and smoothed into C2121. The voltage over C2121 is approximately 300V. It can vary from 100V to 390V.

Start up circuit and Vcc supply
This circuit is formed by R3123, R3134, C2129, D6129, R3129, R3111, C2133 and C2111.
When the power plug is connected to the mains voltage, the stabilised voltage over D6129 (24V) will charge C2133 via R3129. When the voltage reaches 14.5V across C2111, the control circuit of IC7110 is turned on and the regulation starts. During regulation, Vcc of IC7110 will be supplied by the rectified voltage from winding 7-9 via L5132, D6132 and C2133.

Control circuit
The control circuit exists of IC7110, C2102, C2104, C2107, C2109, C2110, R3102, R3103, R3104, R3107, R3108, R3109 and R3110. C2102 and R3110 define the frequency of the oscillator.

Power switch circuit
This circuit comprises MOSFET 7125, Rsense 3126, 3127 and 3128, R3125 , C2127, L5125, R3112 and R3113. R3125 is a pull-down resistor to remove static charges from the gate of the MOSFET.

Regulation circuit
The regulation circuit comprises opto-coupler 7200 which isolates the error signal from the control IC on the primary side and a reference component 7201. The TL431(7201) can be represented by two components:
a very stable and accurate reference diode
a high gain amplifier

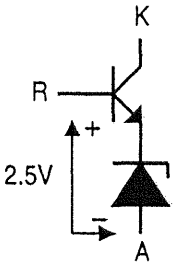

Figure 8-17 'TL 431'

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero. The cathode current flows through the LED of the opto-coupler. The collector current of the opto-coupler flows through R3106, producing an error voltage, connected to voltage feedback pin 14 of IC7110.

Demagnetisation
The auxiliary winding (7-9) voltage is used to detect magnetic saturation of the transformer core and connected via R3101 to pin 8 of IC7110. During the demagnetisation phase, the output will be disabled.

Overvoltage protection circuit
This circuit consist of D6114, C2114, R3115 and R3116.
When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed at the auxiliary winding 7-9.
When an overvoltage longer than 2.0 (s is detected, the output is disabled until VCC is removed and then re-applied. The power supply will come in a hiccup mode as long as the error in the control loop is present.

Secondary rectifier/smoothing circuit
There are 5 rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.
The -8V supply is regulated by voltage regulator 7249.

On/off circuit
In off mode pin 1 and pin 2 of connector 0206 are connected. The high voltage (-8V, +12V) over opto coupler 7200 forces this one to conduct. IC7110 is switched off and thus the output supply voltages.

8.2.2 Troubleshooting PSU 20PS317

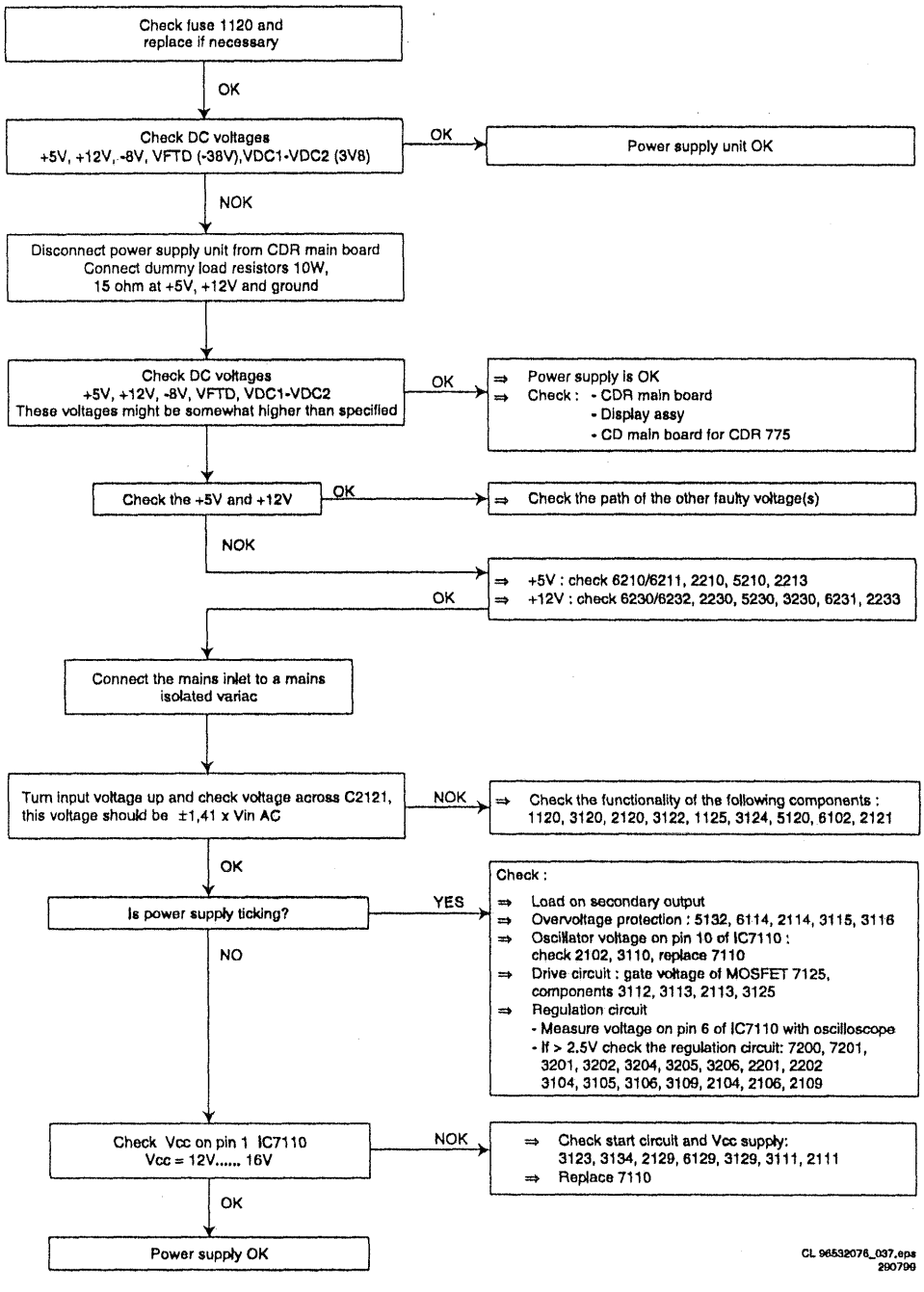

Figure 8-18

8.3 CD Main Board

The CD main board is built around the compact disc mechanism VAM1250 and a loader 1250. The CDM delivers diode signals and an unequalised high frequency signal. These signals are necessary inputs for the decoder CD10. Based on these signals the decoder will control the disc. The decoder is able to control the sledge, focus motor, radial motor and turn table. When everything is "locked", the decoder delivers a digital output according to IEC958 standard, subcode to the microprocessor and I2S for reproducing analog audio signals by means of a D/A converter.

The microprocessor controls the CD10 and is slave of the master processor on the CDR main board in the CDR775. Both processors communicate via a DSA connection (data, strobe and acknowledge).

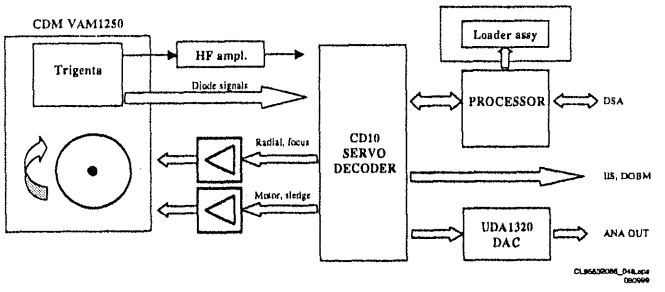

Figure 8-19

8.3.1 Supply Voltages

Description

The CD main board receives +5V and +12V from the CDR main board via respectively pin 16 and pin 15 of connector 1208. The +5V is split up into +5VHF and +5V. The +5VHF is used mainly for the diode currents and the HF-amplifier. The +5V is used for the digital part of the board. On the board a +3V3 is made from the +5V for the decoder CD10 and an A3V3 for the DAC UDA1320. The +12V is split up into A12V for the audio output stage and +12V for the power drivers of the CDM.

Measurements

Connect following supplies to next pins :

- +5V + 5% to pin 16 of connector 1208.
- +12V + 5% to pin 15 of connector 1208.
- Ground reference to pin 17 of connector 1208.

Keep microprocessor 7202 in reset by forcing pin 7 of connector 1208 to +5V. Check the following voltages :

Point	Voltage
Position 1000 pins 1,3	+5V ± 5%
Position 7000 pins 5,17,21,57	+3.3V ± 5%
Position 7005 pin 14	+5V ± 5%
Position 7020 pins 25	+5V ± 5%
Position 7020 pins 26,27,28	+10 ± 10%
Position 7021 pin 5	+12V ±10
Position 7022 pin 5	+12V ±10
Position 7025 pin 16	+5V ± 5%
Position 7202 pin 38	+5V ± 5% (other appl. 3V3 possible)
Position 7309 pins 4,13	+3V3 ± 5%
Position 7120 pin 8	+12V ± 10

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Figure 8-20

8.3.2 Clock Signals

Description

The microprocessor has its own Xtal or resonator of 12MHz. The CD10 needs a clock of 8.4672MHz + 100ppm. This speed also relates to the disc speed. To avoid locking problems between the two drives in the CDR775, both drives run on the same clock. Therefore the CD main board gets the clock for the decoder from the CDR main board via pin 2 of connector 1208. The DAC needs a system clock to drive its internal digital filters and to clock the I2S signals from the decoder. In our case this is 11.2896MHz (CL11) generated by the CD10.

Measurements

- Connect the power supply as described above in "1.1.1. Supply Voltages".
- Connect on pin 2 of position 1208 a clock signal of 8.4672 MHz (100ppm minimum rise time of 50ns and at TTL level (0V and +5V).
- Keep microprocessor 7202 in reset by forcing pin 7 at position 1208 to +5V.
- Release the reset. Now, the processor will reset the CD10 for at least 75µs.
- The output clock CL11 should be available now at pin 42 of the CD10.

Check the following frequencies :

Point	Frequency
Position 7000 pin 16	8.4672 MHz ± 100ppm
Position 7202 pins 14,15	12MHz ± 5%
Position 7309 pin 6	11.2896 MHz ± 100ppm
Position 7309 pin 1	2.1168 MHz ± 100ppm
Position 7309 pin2	44.1kHz ± 100ppm

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Figure 8-21

8.3.3 CD10 Decoder/Servo SAA7324 (7000)

Description

The CD10 is a single chip combining the functions of a CD decoder, digital servo and bitstream DAC. The decoder/servo part is based on the CD7. The decoding part supports a full audio specification and can operate at single speed (n=1) and double speed (n=2).

Block Diagram

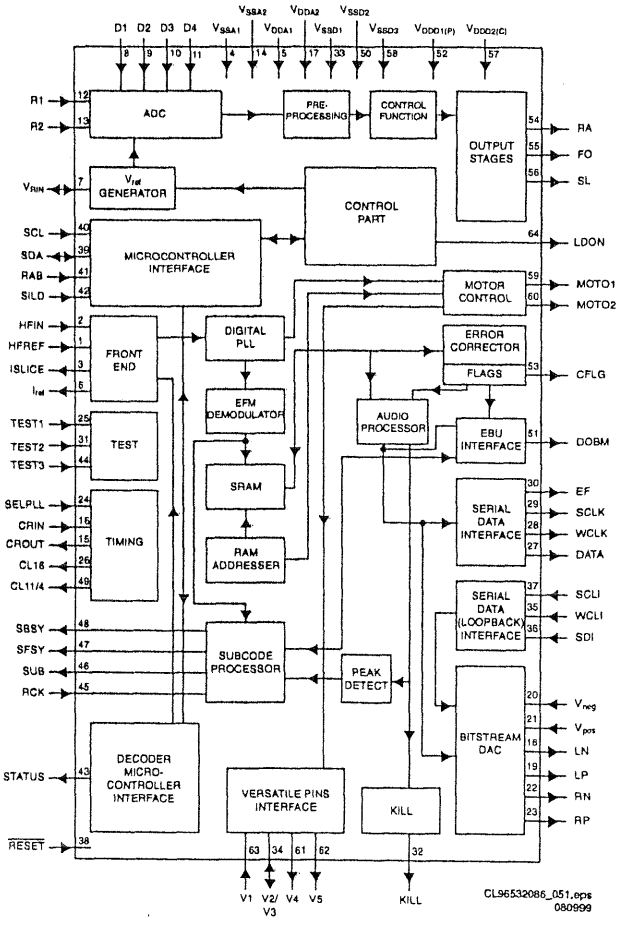

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Figure 8-22

Pin Configuration

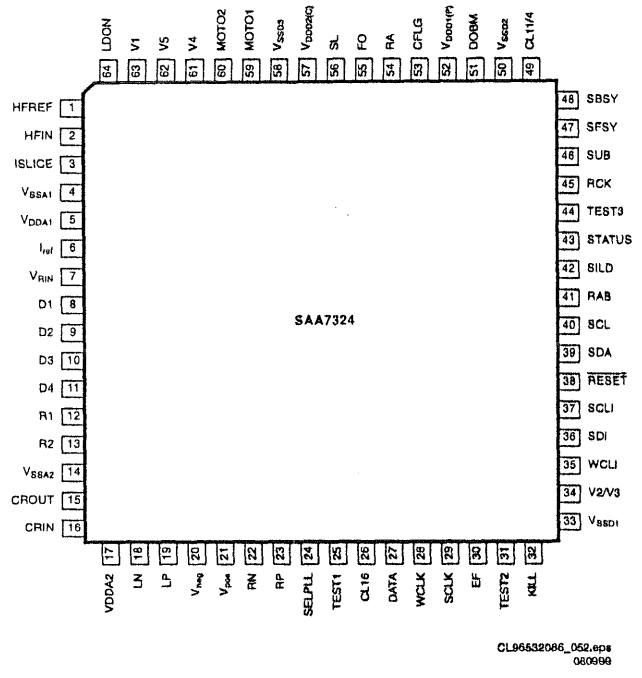

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Figure 8-23

8.3.4 TDA7073A Power Drivers (7021, 7022)

Description

The TDA7073A is a dual power driver circuit for servo systems with a single supply. In this configuration it is used to drive the sledge, tray, focus and radial.

Measurements

Keep microprocessor 7202 in reset by forcing pin 7 of connector 1208 to +5V. Connect the power supply as described above in "1.1.1. Supply Voltages". Check the following voltages :

Pin	Location	Value
5	7021	12V ± 10%
5	7022	12V ± 10%
1	7022	1.65V ± 10%
2	7022	1.65V ± 10%
6	7022	1.65V ± 10%
7	7022	1.65V ± 10%
1	7021	5.0 ± 10%
2	7021	5.0 ± 10%
6	7021	1.65V ± 10%
7	7021	1.65V ± 10%

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Figure 8-24

Pin	Location		Value DC
9	7022	FOC	5.8V ± 10%
12	7022	FOC	5.8V
13	7022	RAD	5.8V
16	7022	RAD	5.8V
9	7021	SLE	5.8V
12	7021	SLE	5.8V
13	7021	TRAY-	5.8V
16	7021	TRAY+	5.8V

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Figure 8-25

8.3.5 BA6856FP Turn Table Motor Driver (7020)

Description

This component is a 3 phase, full wave pseudo linear driving system with inbuilt Hall Bias circuit and 3 phase parallel output.

Measurements

Keep processor 7202 in reset by forcing pin 7 of connector 1208 to +5V. The outputs 9, 10, 11 of connector 1006 are 0V.
Pin 21 of the motor driver 7020 is 2.5V (10%.
Pin 22 of the motor driver 7020 is 2.5V (10%.
Pin 23 of the motor driver 7020 is 0V.
Pin 19 of the motor driver 7020 is 5V (10%.
Put the processor out of reset to continue the measurement.
Check MOT1 at pin 59 of CD10. The duty cycle of the output should be 50%. Check wave form at pin 11 of 7005-D : amplitude 5V + 5% duty cycle 50%.
The motor driver 7020 can be measured dynamically by connecting a hall motor to the application panel. Apply a pulse of 1V 10Hz and 15% duty cycle to pin 22 (Ec) as input value with reference to pin 21 (Ecr=2.5V). Measure the output signals on the driver. This will give as response a square wave on pin 17 and pin 18. When a positive voltage is applied, the square wave on pin 17 will go ahead of the square wave on pin 18. All signals will have a value as shown in the truth table. Check the following output signals :

Motor controller truth table

Input conditions conn 1006 pin						Outputs conn 1006			Test points on driver		
6	8	4	7	3	2	9	10	11	18	17	16
U+	U-	V+	V-	W+	W-	UCOIL	VCOIL	WCOIL	HALL_U	HALL_V	HALL_W
L	M	H	M	M	M	6V	0V	0V	0V	5V	
H	M	L	M	M	M	0V	6V	6V	5V	0V	
M	M	L	M	H	M	0V	6V	0V		0V	5V
M	M	H	M	L	M	6V	0V	6V		5V	0V
H	M	M	M	L	M	0V	0V	6V	5V		0V
L	M	M	M	H	M	6V	6V	0V	0V		5V

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Figure 8-26

Hall-elements input signal voltage levels

Input voltage	Level	Tolerance	Unit
H	2.8	0.1	V
M	2.5	0.1	V
L	2.2	0.1	V

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Figure 8-27

8.3.6 Tray Control

Description

The tray control consists of a TDA7073A power driver (7021) controlled by the processor 7202 via pin 19 TRAYIN and pin 20 TRAYOUT. If pin 20 is low and pin 19 high, the TRAY+ signal at pin 16 of 7021 is forced to +8V and the TRAY- signal at pin 13 of 7021 to GND : the tray will open. If pin 20 is high and pin 19 low, TRAY+ becomes GND and TRAY- becomes +8V : the tray will close. If pin 19 and 20 of the processor have the same value, TRAY+ and TRAY- will have the same value as well : the tray stops moving.

Measurements

Keep procesor 7202 in reset by forcing pin 7 of connector 1208 to +5V. Connect a load of 15Ω, 7W between pin 3 and 4 of connector 1002. Check the voltage over the load with TRAY+ (pin 3) as positive reference. Check also the levels of pins 19 and 20 of the processor.
U TRAY+,TRAY- = <100mV
Pin 20 = +5V
Pin 19 = +5V
Force pin 20 of the processor to ground, and check the voltages.
U TRAY+,TRAY- = -6.5V(10%
Pin 20 = +0V
Pin 19 = +5V
Force pin 19 of the processor to ground as well and check the levels again.
U TRAY+,TRAY- = <100mV
Pin 20 = +0V
Pin 19 = +0V
Release pin 20 of the processor and check the levels.
U TRAY+,TRAY- = 6.5V(10%
Pin 20 = +5V
Pin 19 = +0V
Release pin 19 of the processor and check the levels again:
U TRAY+,TRAY- = <100mV
Pin 20 = +5V
Pin 19 = +5V

8.3.7 HF Path

Description

The pre-amplified HF-signal is presented to both n=1 and n=2 amplifier circuits. The mux/demux switches via software and micro processor controlled S1 and S2 lines between either one of the amplified n=1 or n=2 signals. The signal will then follow another amplification and filtering circuit. The filtering again is controlled by the S1 and S2 lines, dependant on whether the disc starts up (speed n=1, S1 and S2 Low), disc plays at speed n=1 (S1 Low, S2 High) or disc plays at speed n=2 (S1 and S2 High).

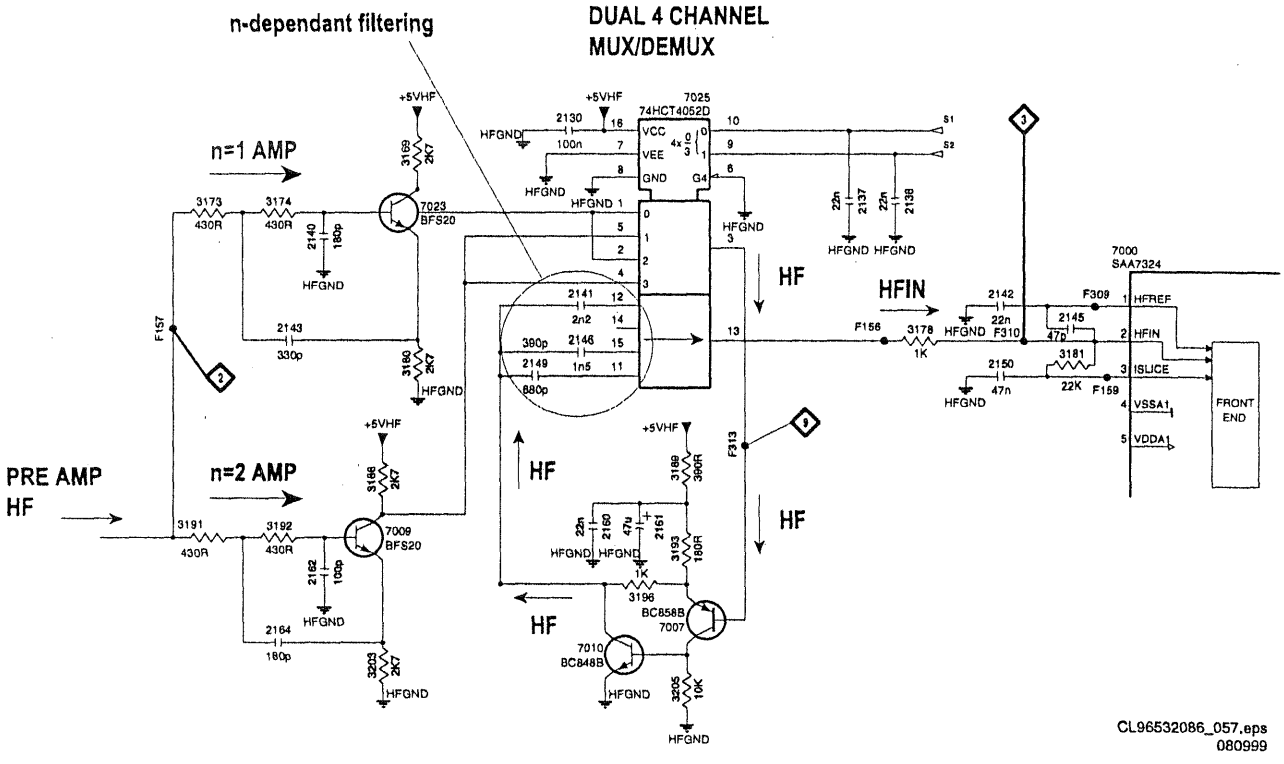

Figure 8-28

DC Settings

Set the power and reset connections as described above in "1.1.1. Supply Voltages". Check the following voltages :

Force	Pin	Location	Measure
	Emitter	7006	2.4 ± 10%
S1 and S2 "HIGH"	Collector	7010	1.9 ± 10%
S1 and S2 "LOW"	Collector	7010	1.9 ± 10%
S1 and S2 "HIGH"	13	7025	1.6 ± 10%
S1 and S2 "LOW"	13	7025	1.6 ± 10%
S1 and S2 "HIGH"	3	7025	3.2 ± 10%
S1 and S2 "LOW"	3	7025	3.2 ± 10%

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Figure 8-29

Transfer Characteristics
Set the power and reset connections as described above in "1.1.1. Supply Voltages". Connect a function generator via a serial resistor of 1k5 to pin 4 of connector 1000. Use the function generator as a sine wave generator with output level of 1Vtt. Check this AC value with an AC mV-meter connected to the input (pin 2) of the CD10 (7000) :

Frequencies	S1 and S2 "low"		S1 and S2 "high"	
	Input V_{AC}	Pin 2 at 7000	Input V_{AC}	Pin 2 at 7000
300 Hz	200mV	< 100mV ± 20%	200mV	< 100mV ± 20%
10 kHz	200mV	295mV ± 20%	200mV	330mV ± 20%
100 kHz	200mV	310 mV ± 20%	200mV	330 mV ± 20%
300 kHz	200mV	385 mV ± 20%	200mV	335 mV ± 20%
800 kHz	200mV	655 mV ± 20%	200mV	485 mV ± 20%
1.5 MHz	200mV	1.1V ± 20%	200mV	760 mV ± 20%
3MHz	200mV	1.1V ± 20%	200mV	1.1V ± 20%

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Figure 8-30

HFDET Setting
Set the power and reset connections as described above in "1.1.1. Supply Voltages". Connect a function generator via a serial resistor of 1k5 to pin 4 of connector 1000. Use the function generator as a sine wave generator with output level of 500 kHz, 1Vtt. Check this AC value with an AC mV-meter :

Location	Voltage DC		Voltage AC
	No HF	HF	
F190	4.8V± 20%	4.8V± 20%	175mV± 20%
F192	< 100mV	1.1V± 20%	-
F206	4.9V± 20%	150mV± 20%	-

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Figure 8-31

8.3.8 Audio Part - DAC

Description
The DAC used, is the UDA1320 bit stream, continuous calibration. I2S signals from various formats can be entered at pins 1,2 and 3. If these signals are in phase with the delivered system clock at pin 6, the DAC will reproduce analog output signals at pins 14 and 16. 0dB level is 0.85Vrms. These analog signals are at 1.65Vdc level.
The DAC has features which can be checked on the input pins. Mute will switch off the analog signals. De-emphasis is not used, since this is done in the decoder. Attenuation of -12dB is not used because this is also done in the decoder.

I2S
I2S is a kind of digital audio format, consisting out of 3 lines : CLOCK, WORDSELECT and DATA.

WORD-SELECT
Word select (WS) indicates whether the data-sample is from the left or the right audio-channel. It has the same frequency as the sample rate of the digital audio signal. This can be 32, 44.1 or 48kHz. Normal polarity is low for a left sample and high for a right sample. So within the low state of the WS-line the data bits for the left channel are transferred, and within the high state the data bits of the right channel are transferred.

CLOCK
The CLOCK signal (CLK) indicates when DataTips must be set, and when DataTips must be read. The frequency depends on the speed of the I2S-bus, but is always a factor of the frequency of the WS-signal. It can be 48x, 64x, 96, 128x.... .In our case it is 48x the sample rate frequency = 2.1168MHz. The signal is in phase with the WS-signal. Transition of the WS always happens on a falling edge of the CLK.

DATA
DATA contains all data-bits. Data bits are set by the transmitting device, and read by the receiving device. The position of the DATA-bits within the WS-signal is very important. There are several formats for this. In our case we always use Philips I2S format, no Japanese or Sony format. The number of data-bits per channel depends on the used devices.

Timing of the I2S-bus, in case of Philips I2S is shown in the next figure :

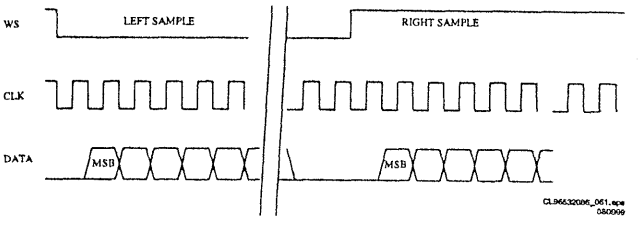

Figure 8-32

Measurements

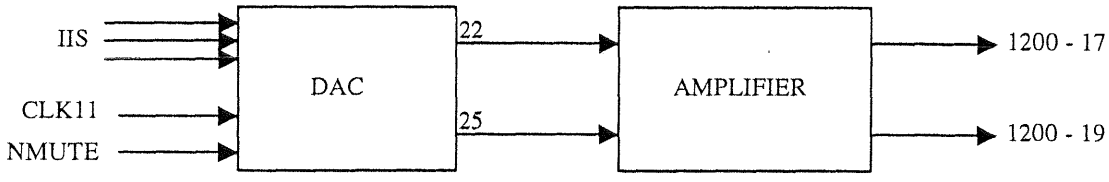

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Figure 8-33

Keep processor 7202 in reset by forcing pin 7 of connector 1208 to +5V. This puts the processor outputs in tristate. Check the reset at pin 4 of processor 7202 to make sure that the processor is in reset.
Now, force port 0-4 pin 33 at 7202 to 0V to set the decoder outputs (SCLK, WCLK, DATA, and CL11).
Check the MUTE pin 11 at 7309 : this pin should be low.
Connect via an I2S generator I2S-signals to the DAC :
Pin 1 at 7309: SLCK.
Pin 2 at 7309: WCLK.
Pin 3 at 7309: DATA.
Connect also the SYSCLK pin 6 at position 7309 to a clock signal of 11.2896 MHz (100ppm.
Generate an I2S signal equivalent with a sine wave of 1kHz at 0dB for both left and right channels.
Check if 0.8 VRMS at pins 14 and 16 at location 7209 with a DC of 1.65VDC.
Check if 1.7 VRMS (2 dB at connector pins 1and 3 at location 1209.
Force MUTE Pin 11 at 7309 high.
Measure again at pins 1 and 3 at location 1209 : both signals should be at -90 dB.

9. List of Abbreviations

SIGNAL NAME	SIGNAL FLOW	FUNCTION AND DESCRIPTION
+12V	main supply voltage from PSU	+12V supply voltage from PSU
+12VA	supply voltage	+12V supply voltage for Audio part
+5V	main supply voltage from PSU	+5V supply voltage from PSU
+5VA	supply voltage	+5V supply voltage for Audio part
+9SRVPWR	IC7558 -> IC7240	PoWeR supply for SeRVo driver IC
12VPWR	supply voltage	+12V supply voltage for servo part
-8V	main supply voltage from PSU	-8V supply voltage from PSU
-8VA	supply voltage	-8V supply voltage for Audio part
A(1:20)	IC7701 -> R3818,R3819, R3820, R3821, R3897 -> IC7703	Address lines 1 to 20 between DASP and flash ROM
A(10:20)	IC7701 -> R3819, R3820, R3821 -> IC7702	Address lines 10 to 20 between DASP and DRAM
A1	IC7010 -> IC7270	amplitude of the "land" reflection relative to the average EFM, voltage output, OPC input
A1LF, A2LF	CONN1000 -> IC7010	satellite photo diodes A1, A2 current output
A2	IC7010 -> IC7270	amplitude of the "pit" reflection relative to the average EFM, voltage output, OPC input
A-8V	supply voltage	-8V supply voltage for servo part
AEGER		Analog Error signal GEnerator for Recordable
AINTON	IC7008 -> IC7010	Alpha INTegrator ON (to AEGER)
ALE	IC7270 -> R3213 -> IC7209, IC7300IC7270 -> R3230	Address Latch Enable; external address latch strobe line, freeze address when low
ALPHA0	IC7270 -> IC7010	analog voltage mode output from OPC D/A converter
ALS	IC7008 -> IC7010	Alpha Loop Switch (to AEGER)
ASTROBE	IC7008 -> IC7010	Alpha STROBE (to AEGER)
ATIP		Absolute Time In Pre-groove (sync signal)
ATIPSYNC	IC7300 -> IC7270	ATIP SYNC signal
ATT	IC7270 -> R3717, R3722IC7270 -> IC7701	ATTenuation request from MACE2 to audio DAC, active low; means that the output can be attenuated in case of search activities
B1LF, B2LF	CONN1000 -> IC7010	satellite photo diodes B1, B2 current output
BCLK	IC7701 -> R3898A -> IC7300	I2S1 BitCLocK from DASP to CDR60 (playback and record)
BE_RESET	IC7701 -> R3261 -> IC7270IC7701 -> R3716	Basic Engine RESET, active high
BIASC	IC7008 -> R3056	BIAS Current switch CDRW output
BKPT	CONN1819, R3907 -> IC7701	JTAG mode select / debug mode BreaKPoinT
C1LF, .. , C4LF	CONN1000 -> IC7010	Central photo diodes C1, C2, C3, C4 current output
CAGAIN	R3016,R3115 -> IC7010	set-point laser power on disc, current input
CAHF	CONN1000 -> C2374	Central Aperture (central photo diodes) High Frequency current output (C1+C2+C3+C4)
CALF	IC7010 -> IC7270	Central Aperture (central photo diodes) Low-pass Filtered signal (DC coupled EFM signal), voltage output, OPC input
CAS0	IC7701 -> IC7702	Column Address Strobe DRAM for upper byte
CAS1	IC7701 -> IC7702	Column Address Strobe DRAM for lower byte
CDR	IC7008 -> IC7355	CDR strategy detected output (active high)
CDR60CFLG	IC7300 -> R3382B -> CONN1812	serial output of error corrector status information of the CDR60-decoder, to be measured at test connector
CDR60CL1	IC7300 -> R3382C -> CONN1812	output of CLock signal for testing system clock of IC CDR60 at test connector
CDR60CS	IC7270 -> R3235B -> R3702, IC7300	CDR60 Chip Select, active high
CDR60INT	IC7300 -> IC7270	CDR60 INTerrupt line, active low
CDR60LWRT	IC7300 -> R3048	CDR60 Laser WRiTe control output

CDR60MEAS1	IC7300 -> R3382A -> CONN1812	serial output of information about jitter, PLL frequency and asymmetry of bit recovery block in CDR60, to be measured at test connector
CDR60PLL	IC7270 -> R3305 -> IC7300	CDR60 clock multiplier enable, active high
CDRW	IC7355D -> IC7355CIC7355D -> CONN1000	inverted CDR-strategy-detected signal
CLK_OUT	IC7701 -> R3771 -> CONN1819	system CLocK OUT
CLK_SYS	IC7701 -> R3727, R3731	oscillator output
COS-	CONN1220 -> IC7225B	Hall feedback signal from sledge motor
COS+	CONN1220 -> IC7225B	Hall feedback signal from sledge motor
CSFLASH	IC7701 -> IC7703	Chip Select for FLASH or boot device
CSRAM	IC7270 -> R3235A -> R3703, IC7802	Chip Select SRAM, active low
D(16:31)	IC7701 <-> R3822, R3823, R3824, R3825 <-> IC7703, IC7702	Databus bit 16 to 31 between DASP, flash ROM and DRAM
D3V3	supply voltage	+3,3V supply voltage for Digital part
D5V	supply voltage	+5V supply voltage for Digital part
D5VS	supply voltage	+5V supply voltage for Servo part
DALPHA	IC7010 -> R3037	ALPHA error signal for laser power control
DASP		Digital Audio Signal Processor
DATAI	IC7701 -> R3898C -> IC7300	I2S1 DATA In from DASP to CDR60 (recording)
DATAO	IC7300 -> R3314 -> IC7701	I2S1 DATA Out from CDR60 to DASP (playback)
DEEMP	IC7270 -> R3719, R3724IC7270 -> IC7701	DE-EMphasis control for audio DAC from MACE2, active high; means that de-emphasis is needed in digital filter
DELTAP	IC7016 -> R3126	DELTA Power current source drive signal from XDAC
DIG_OUT_C	IC7701 -> R3706 -> C2707, CONN1400	Common DIGital OUTput (consumer)
DISPLAY_INT	F934 -> R3812, IC7701	DISPLAY INTerrupt
DMON	IC7270 -> R3324	power save at stop, active low
DOBM_CD	CONN1708, C2731 -> R3757 -> R3903 -> IC7701	Digital Output (EBU output) from CD player in CDR775 to DASP
DOBM_CDR	IC7300 -> R3382D -> C2379, IC7701	Digital Output (EBU output) from CDR60 to DASP
DRAM_RW	IC7701 -> IC7702	Read/Write strobe for DRAM
DSA_ACK_CD	IC7701 <-> R3830 <-> R3831 <-> CONN1708IC7701 <-> R3830 <-> C2735	Data/Strobe/Acknowledge serial communication between DASP and CD-player in CDR775
DSA_ACK_CDR	IC7701 -> R3729 -> IC7270, CONN1830IC7701 -> R3729 -> R3769	Data/Strobe/Acknowledge serial communication between MACE2 and DASP for CDR; acknowledge input for MACE2 is strobe output for DASP
DSA_DATA_CD	IC7701 <-> R3828 <-> R3829 <-> CONN1708IC7701 <-> R3828 <-> C2733	Data/Strobe/Acknowledge serial communication between DASP and CD-player in CDR775
DSA_DATA_CDR	IC7270<->R3246 <-> R3813 <-> IC7701, CONN1830IC7270<->R3246 <-> R3767	Data/Strobe/Acknowledge serial communication between MACE2 and DASP for CDR
DSA_STR_CD	IC7701 <-> R3835 <-> R3832 <-> CONN1708IC7701 <-> R3835 <->C2734	Data/Strobe/Acknowledge serial communication between DASP and CD-player in CDR775
DSA_STR_CDR	IC7270 -> R3245 -> IC7701, CONN1830IC7270 -> R3245 -> R3768	Data/Strobe/Acknowledge serial communication between MACE2 and DASP for CDR (strobe output for MACE2 is acknowledge input for DASP)
DSCLK	CONN1819, R3908 -> IC7701	reset in / Debug Serial CLocK in
DSI	CONN1819, R3909 -> IC7701	JTAG reset in / Debug Serial clock In
EFM		Eight to Fourteen Modulation = modulation method used for CD storage, also the actual raw CD signal as written or read on or from the CD disc
EFMCLK	IC7300 -> IC7008	EFM CLocK output
EFMDATA	IC7300 -> IC7008	EFM DATA output
EFMTIM3		EFM TIMing generator
EPON	IC7008 -> R3010IC7008 -> C2010	Erase Power ON
EPONO	IC7008 -> R3107	Erase Power ON Open drain output
EPONRC	R3004 -> CONN1000	Erase Power ON (after RC circuit)

ERASEC	IC7008 -> R3087	ERASE Current switch CDRW output
ERON	IC7008 -> IC 7010	ERror ON (to AEGER)
EXT_DIG_IN1	CONN1400 -> IC7701	EXTernal DIGital INput 1
EXT_DIG_IN2	CONN1702, C2767, C2721 -> R3701 - >IC7701	EXTernal DIGital INput 2 (CDR950 only)
EXT_OPT_IN	CONN1400, C2722 -> R3708 -> IC7701	EXTernal OPTical INput
F_READY	IC7703 -> R3817 -> IC7701CONN1701 - > IC7701	Flash READY detection, this line is forced low as long as the flash is busy with erase or program algorithm
F_RW	IC7701 -> IC7708B	Read/Write strobe for Flash ROM
FEN	IC7010 -> IC7270	Focus Error Normalized current output
FOC-	IC7240 -> CONN1000	FOCus actuator drive signal negative connection
FOC+	IC7240 -> CONN1000	FOCus actuator drive signal positive connection
FS30V	D6500 -> CONN1000	Forward Sense diode 30V power supply
FSA	CONN1000 -> T7119, T7120	Forward Sense photo diode current output
FSCLR	IC7008 -> IC7126	Forward Sense signals CLeaR switch
FSOF	IC7008 -> R3052	Forward Sense photo diode sampling OFf
FSON	IC7008 -> R3051	Forward Sense photo diode sampling ON
FSR	R3040 -> IC7270	Forward Sense signal while Reading for read control loop
FSRS	IC7008 -> IC7126D	Forward Sense photo diode Read Sampling
FSW	R3050 -> IC7270	Forward Sense signal while Writing for write control loop
FSWS	IC7008 -> IC7126C	Forward Sense photo diode Write Sampling
FWEN	IC7270 -> IC7208, R3806	Flash EPROM Write ENable
HALL_U, HALL_V, HALL_W	IC7330 -> IC7300, CONN1812	HALL feedback signals from turn table motor via hall motor driver
HFS0	IC7270 -> R3249 -> IC7360	select HF circuit
I2C		Inter IC
I2C_CLK	IC7701, R3711 -> R3715 -> C2709 -> F934IC7701, R3711 -> IC7801	I2C CLocK line used for display slave processor and digital potmeter
I2C_DATA	IC7701, R3712 <-> R3713 <-> C2708, R3714 <-> F934IC7701, R3712 <-> IC7801	I2C DATA line used for display slave processor and digital potmeter
I2CL	R3248B -> IC7207, R3247C	I2C CLock line
I2CSCL	IC7207 -> IC7008IC7207 -> IC7010IC7207 -> R3248B	I2C Serial CLock line
I2CSDA	IC7207 <-> IC7008IC7207 <-> IC7010IC7207 <-> R3248A	I2C Serial DAta line
I2DA	R3248A <-> IC7270,R3247D	I2C DAta line
I2S_BCLK_AI	IC7701 -> R3814 -> IC7406	I2S4 Bit CLocK for CODEC (ADC for CDR950) Analog Input (record from analog source)
I2S_BCLK_AO	IC7701 -> R3894A -> IC7406	I2S2 Bit CLocK for CODEC (DAC for CDR950) Analog Output
I2S_BCLK_CD	CONN1708, C2739 -> R3834 -> IC7701	I2S3 Bit CLocK from CD player (record n=2) (CDR775 only)
I2S_BCLK_MIC	CONN1708, C2739 -> R3834 -> IC7701	I2S3 Bit CLocK from MICrophone (CDR950 only)
I2S_DATA_AI	IC7406 -> IC7701	I2S4 DATA from CODEC (ADC for CDR950) Analog Input (record from analog source)
I2S_DATA_AO	IC7701 -> R3894C -> IC7406	I2S2 DATA for CODEC (DAC for CDR950) Analog Output
I2S_DATA_CD	CONN1708, C2738 -> R3836 -> IC7701	I2S3 DATA from CD player (record n=2) (CDR775 only)
I2S_DATA_MIC	CONN1708, C2738 -> R3836 -> IC7701	I2S3 DATA from MICrophone (CDR950 only)
I2S_WS_AI	IC7701 -> R3743 -> IC7406	I2S4 Word CLocK for CODEC (ADC for CDR950) Analog Input (record from analog source)
I2S_WS_AO	IC7701 -> R3894B -> IC7406	I2S2 Word CLocK for CODEC (DAC for CDR950) Analog Output
I2S_WS_CD	CONN1708, C2740 -> R3833 -> IC7701	I2S3 Word CLocK from CD player (record n=2) (CDR775 only)
I2S_WS_MIC	CONN1708, C2740 -> R3833 -> IC7701	I2S3 Word CLocK from MICrophone (CDR950 only)
I2S1_MS	IC7270 -> R3910, IC7701	I2S1 Master-Slave interrupt from MACE2
IE	T7121 -> CONN1000	laser Erase drive current signal

INT_COPY_ANA	IC7701 -> R3721 -> IC7401IC7701 -> R3721 -> R3410	select INTernal COPY ANAlog (in case of copy protected disc or track on CD drive) (CDR775 only)
IR	T7135 -> CONN1000T7135 -> R3056T7135 -> IC7008	laser Read drive current signal
IW	T7122 -> CONN1000T7122 -> D6003	laser Write drive current signal
KEY_PRESSED	IC7706B -> R3816 -> IC7701	KEY PRESSED interrupt
KILL	T7560, T7561, R3560 -> CONN1400, R3424, R3428	KILL signal from power supply part to audio outputs
KILL_OUT	IC7701 -> R3532	disables the KILL activity from the PSU; 1 = no kill,0 = kill active
L12V	supply voltage	+12V supply voltage for servo/Laser part
L3_CLK	IC7701 -> R3725 -> IC7406	L3 interface CLocK line / control CODEC (not for CDR950)
L3_DATA	IC7701 <-> R3728 <-> IC7406	L3 interface DATA line with CODEC (not for CDR950)
L3_MODE	IC7701 -> R3735 -> IC7406	L3 interface MODE line selects data or address transfer mode for CODEC (not for CDR950)
L5V	supply voltage	+5V supply voltage for servo/Laser part
L-5V	supply voltage	-5V supply voltage for servo/Laser part
LASCK	IC7270 <-> R3248D	ClocK line DAC LASer control
LASDACCK	R3248D <-> IC7016	ClocK line DAC LASer control
LASDACDI	R3248C <-> IC7016	Data line DAC LASer control
LASDACLD	R3212 <-> IC7016	LoaD line DAC LASer control
LASDD	IC7270 <-> R3248C	Data line DAC LASer control
LASLD	IC7270 <-> R3238 <-> R3212IC7270 <-> R3232	LoaD line DAC LASer control
LEFT	CONN1708, C2743 -> IC7401C, IC7407C	audio output LEFT channel from CD-player in CDR775
LLP	IC7270 -> IC7300	Laser Low Power (active high), switches the laser from write to read power whenever the device tends to go offtrack
LWRT	R3048 -> IC7008	Laser WRiTe control input
MA(16:17)	IC7270 <-> IC7208	bank switch higher address lines
MA(8:15)	IC7270 <-> IC7802 <-> IC7208	address bus high byte
MACE2		Mini All Cd Engine (minus decoder + OPC + PCS + extra RAM)
MAD(0:7)	IC7270 <-> IC7209 <-> IC7802 <-> IC7208 <-> IC7300	bi-directional data bus / address bus low byte
MIRN	IC7010 -> IC7270	MIRror Normalized (disc reflection) current output
MOTO1	IC7300 -> IC7355A	turn table MOTOr control output
MRDN	IC7270 -> R3276 -> R3242A, IC7802, IC7300	Master ReaD, read strobe for external peripherals, active low
MUTE	IC7270 -> R3718, R3723IC7270 -> IC7701	MUTE control from MACE2 to DASP, active low
MWRN	IC7270 -> R3280 -> R3242B, IC7802, IC7300	Master WRite, write strobe for external peripherals, active low
NMUTE	IC7701 -> R3726, IC7406	MUTE output, low active
OFFTRACK	IC7270 -> IC7300	OFFTRACK detection flag
OPC		Optimum Power Calibration
P12VKILL	supply voltage	+12V supply voltage for KILL-circuit
PCS		Position Control Sledge
PCSCOS	IC7225B, C2229 -> IC7270, CONN1812	Position Control Sledge COS feedback signal
PCSSIN	IC7225A, C2227 -> IC7270, CONN1812	Position Control Sledge SIN feedback signal
PDAR		Photo Diode Amplifier Recordable
PERASE	R3036, R3031, R3030, R3029, R3028, R3027, R3020 -> IC7002C, R3043, T7113	laser Power switch for ERASE
POWER_UP	IC7270 -> R3243C,R3556, R3538	standby pin, high level activates essential powers necessary for full function; overrules HI_POWER setting
PPN	IC7010 -> IC7050C	Push-Pull signal, Normalized, balanced, voltage output

PRCOARSE	IC7016 -> R3057	drive signal from Power Read COARSE DAC for read current source
PRFINE	IC7016 -> R3058	drive signal from Power Read FINE DAC for read current source
PROF_EBU	IC7701 -> CONN1820	PROFessional digital output (CDR950 only)
PSENn	IC7270 -> R3260 -> IC7208IC7270 -> R3231	Program Store ENable; external ROM output enable line, active low
PW	R3081 -> IC7008	Write Power signal to OPC input of MACE2
PWB	IC7001C -> IC7016	drive signal to XDAC<->s for write and erase current sources and VCAGAIN
PWD	IC7016 -> IC7002BIC7016 -> IC7002C	drive signal from XDAC for write and erase current sources
PWMAX	IC7016 -> R3073	PW MAXimum signal from DAC used for determining set point for laser power during writing
PWMIN	IC7016 -> R3072	PW MINimum signal from DAC used for determining set point for laser power during writing
PWRITE	R3035, R3026, R3025, R3024, R3023, R3022, R3021 -> IC7002B, R3044, T7124	laser Power switch for WRITE
RAD-	IC7240 -> CONN1000	Radial actuator drive signal negative connection
RAD+	IC7240 -> CONN1000	Radial actuator drive signal positive connection
RAS0	IC7701 -> IC7702	Row Address Strobe DRAM
RCK	IC7300 -> R3319 -> IC7701	EIAJ subcode clock from CDR60 to DASP (CD text interface)
RDGAIN1	IC7008 -> R3054	forward sense ReaD GAIN switch 1
RDGAIN2	IC7008 -> C2027	forward sense ReaD GAIN switch 2
RDGAIN3	IC7008 -> C2060	forward sense ReaD GAIN switch 3
RE	IC7010 -> IC7215A	Radial Error signal for fast track counting, voltage output
RECORDING	IC7008 -> IC7010IC7008 -> CONN1000IC7008 -> IC7355C	RECORDING output (active high)
REN	IC7010 -> IC7270	Radial Error Normalized current output
RIGHT	CONN1708, C2742 -> IC7401A, IC7407A	audio output RIGHT channel from CD-player in CDR775
RXD_TOOL	CONN1818 -> IC7701	Receive of UART for test TOOL
S1V65	Referenve Voltage	1.65V delivered by IC7215B for Servo part
S2V9	Reference Voltage	2.9V delivered by IC7010 for Servo part
SEL_HP_OUT	IC7701 -> R3720 -> IC7407	SELect HeadPhone OUTput in DJ-mode (for CDR775 only)
SFSY	IC7701 -> R3756 -> IC7300	EIAJ subcode synchronisation from DASP to CDR60 (CD text interface)
SIN-	CONN1220 -> IC7225A	Hall feedback signal from sledge motor
SIN+	CONN1220 -> IC7225A	Hall feedback signal from sledge motor
SL-	IC7240 -> R3265 -> CONN1220	SLedge motor drive signal negative connection
SL+	IC7240 -> CONN1220	SLedge motor drive signal positive connection
SRSTN	IC7270 -> R3243B, IC7300	Slave ReSeT out (CDR60 reset), active low
STANDBY	IC7270 -> R3807 -> R3887 -> IC7701	STANDBY pin, high level activates essential powers necessary for full function; overrules HI_POWER setting
SUB	IC7701 -> R3710 -> IC7300	EIAJ subcode data from DASP to CDR60 (CD text interface)
SYS_CLK_11W	IC7701 -> R3732 -> IC7406	11.2896 MHz SYStem CLocK for AD/DA datapath
SYS_CLK_16W	IC7701 -> R3894D-> IC7706A	16.9344 MHz SYStem CLocK for producing SYS_CLK_BE
SYS_CLK_8W	IC7706A -> R3815 -> CONN1708	SYstem CLocK CD player (8.4672 MHz) (CDR775 only)
SYS_CLK_BE	IC7706A -> R3826 -> IC7270	SYstem CLocK Basic Engine (8.4672 MHz)
SYS_RESET	IC7701 -> R3758 -> CONNF934IC7701 -> R3770 -> T7707 -> CONN1708	SYStem RESET to display assy (and CD player for CDR775)
TCK	CONN1819 -> R3906, IC7701	JTAG ClocK signal
TDSO	IC7701 -> CONN1819	JTAG Serial Data Out / debug data out
TERMB	IC7270 <-> CONN1818	UART connection with MACE
TLN	IC7010 -> IC7270	Track Loss Normalized current output
TR-	IC7240 -> CONN1200	TRay motor drive signal negative connection
TR+	IC7240 -> CONN1200	TRay motor drive signal positive connection

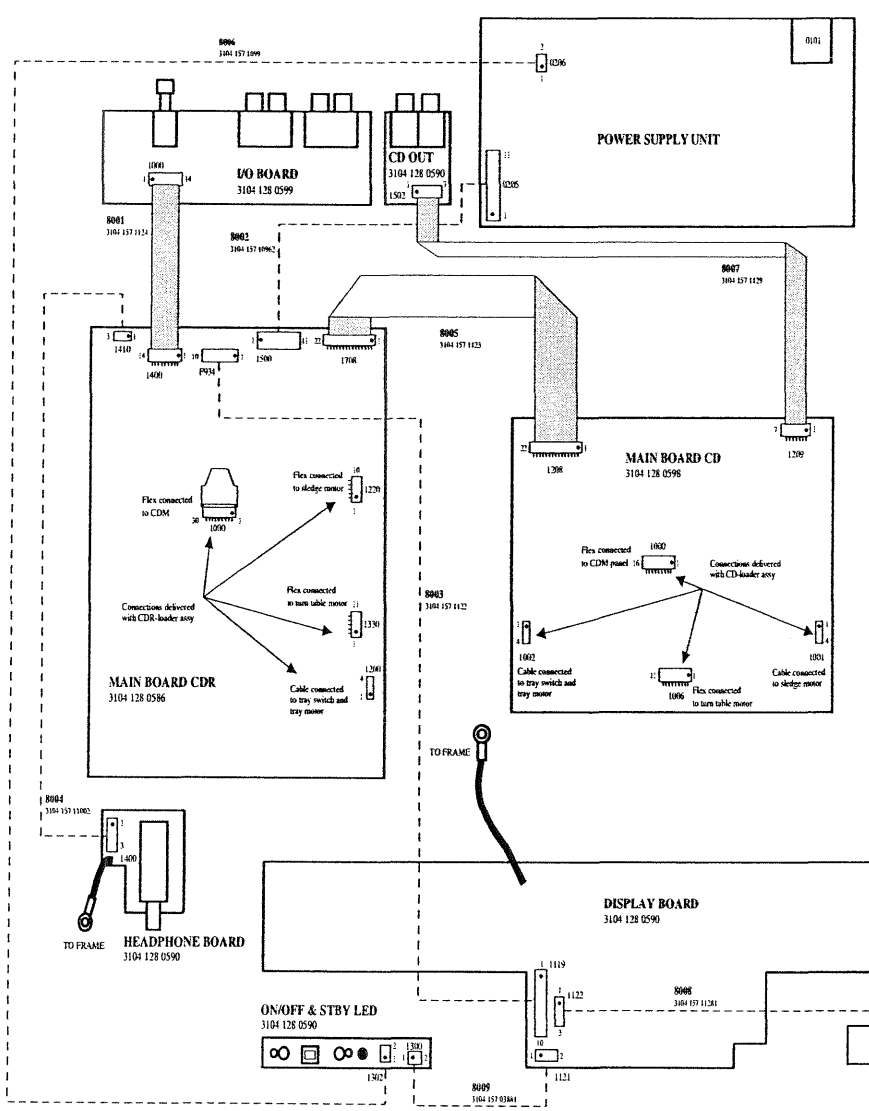
TRACE99_RXD	CONN1818 -> R3838, IC7701	TRACE99 test tool receive data
TRACE99_TXD	IC7701 -> CONN1818	TRACE99 test tool transmit data
TRAYIN	IC7270 -> IC7240	move TRAY IN line, active low
TRAYOUT	IC7270 -> IC7240	move TRAY OUT line, active low

TRAYSW	CONN1200 -> R3747CONN1200 -> R3748	TRAY SWitch signal from loader assy
TRAYSWF	R3748, C2214 -> IC7270	Filtered TRAY SWitch signal, low is completely out or in
TXD_TOOL	IC7701 -> CONN1818	Transmit of UART for test TOOL
U+, U-, V+, V-, W+, W-	CONN1330 -> IC7330	hall feedback signals from turn table motor to hall motor driver
UCOIL, VCOIL, WCOIL	IC7330 -> CONN1330	drive signals for turn table motor
VCAGAIN	IC7016 -> IC7005A	set-point laser power on disc, voltage output
VDC1	CONN1500 -> CONNF934	supply voltage for display assy
VDC2	CONN1500 -> CONNF934	supply voltage for display assy
VFO	IC7270 -> R3295 -> R3244	FOcus actuator drive output
VFTD	CONN1500 -> CONNF934	Voltage Fluorescent Tube Display (display assy)
VRA	IC7270 -> R3297 -> R3254	RAdial actuator drive output
VSL	IC7270 -> R3299 -> IC7240	SLedge actuator drive output
WCLK	IC7701 -> R3898B -> IC7300	I2S1 WordCLocK from DASP to CDR60 (playback and record)
WOBBLE	IC7050C -> IC7300	analog WOBBLE signal of pre-groove detected by PPN-signal
WPON	IC7008 -> R3009IC7008 -> C2009	Write Power ON
WPONO	IC7008 -> R3106	Write Power ON Open drain output
WPONRC	R3003 -> CONN1000	Write Power ON (after RC circuit)
XDAC		multiplying DAC

4. Mechanical instructions

Wiring diagram

WIRING DIAGRAM CDR775



Pin 1 indicated by • All Wires are 1/1, except flex 8001, 8005 and 8007

8001 (at conn. 1400 of CDR main board)

1	GROUND
2	DIG_OUT_C
3	GROUND
4	EXT_DIG_IN
5	EXT_OPT_IN
6	GROUND
7	D5V
8	KILL
9	LEFT_IN
10	GROUND
11	RIGHT_IN
12	RIGHT_OUT
13	GROUND
14	LEFT_OUT

8002

1	VDC2
2	VFTD
3	VDC1
4	GROUND
5	+5V
6	+5V
7	GROUND
8	GROUND
9	GROUND
10	+12V
11	-8V

8003 (at conn. F934 of CDR main board)

1	VDC2
2	VFTD
3	VDC1
4	SYS_RESET
5	IIC_DATA
6	GROUND
7	IIC_CLK
8	DISPL_INT
9	GROUND
10	D5V

8004

1	LEFT_HP_OUT
2	GROUND
3	RIGHT_HP_OUT

8006

1	ON!
2	OFF!

8009

1	LED_ON
2	GROUND

8008

1	+5V
2	IR_IN
3	GROUND

8007 (at conn. 1209 of CD main board)

1	RIGHT_CD
2	GND
3	LEFT_CD
4	GND
5	DOBM_CD
6	GROUND
7	KILL

8005 (at conn. 1708 of CDR main board)

1	GROUND
2	DSA_DATA_CD
3	GROUND
4	DSA_STR_CD
5	DSA_ACK_CD
6	GROUND
7	D5V
8	12V_CD
9	GROUND
10	IIS_DATA_CD
11	IIS_WS_CD
12	GROUND
13	IIS_BCLK_CD
14	GROUND
15	DOBM_CD
16	SYS-RESET
17	LEFT_IN_CD
18	GROUND
19	RIGHT_IN_CD
20	KILL
21	SYS_CLK_8W
22	GROUND

Texture indicates text on flex.

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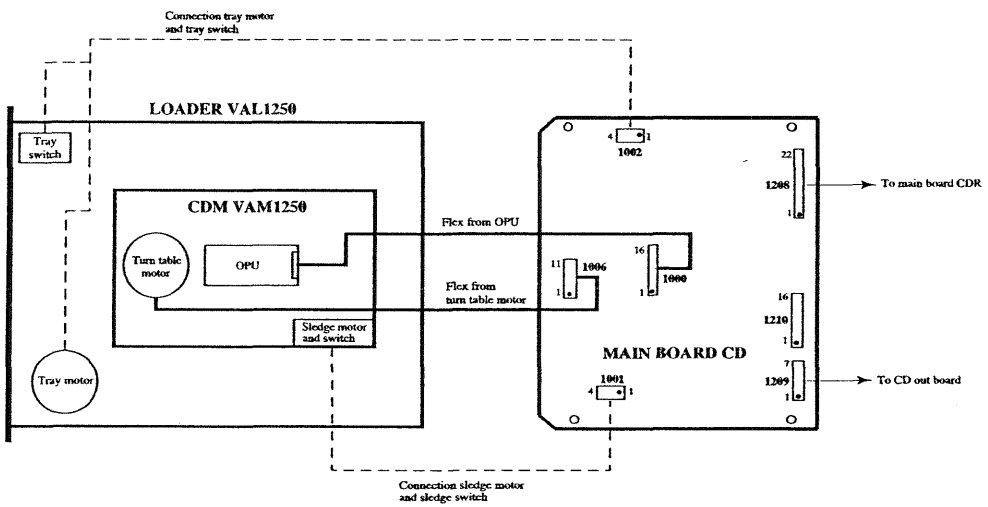
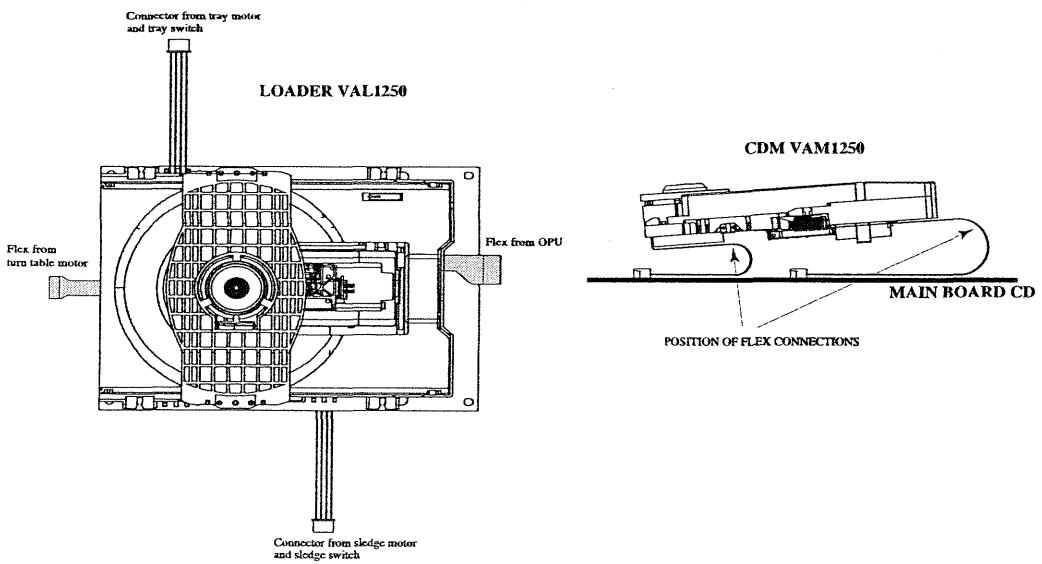
Wiring CD

WIRING DIAGRAM CD LOADER VAL1250





CONNECTOR 1006

1	HALL +
2	W-
3	W+
4	V+
5	HALL-
6	U+
7	V-
8	U-
9	UCOIL
10	VCOIL
11	WCOIL

CONNECTOR 1000

1	VSUB
2	HFGND
3	VDD
4	RF
5	LDON
6	R2
7	R1
8	D4/D3
9	D2
10	D1
11	FTC
12	RW
13	FOC+
14	FOC-
15	RAD+
16	RAD-

CONNECTOR 1002

1	HOMESW
2	SGND
3	TRAY+
4	TRAY-

CONNECTOR 1001

1	HOMESW
2	SGND
3	SL-
4	SL+

CONNECTOR 1209

1	AUDIO R (RIGHT_CD)
2	GND
3	AUDIO L (LEFT_CD)
4	GND
5	DOBM5_CD (DOBM_CD)
6	GND
7	KILL

CONNECTOR 1208

1	GND
2	CRIN (SYS_CLK_8W)
3	KILL
4	AUDIO R (RIGHT_IN_CD)
5	GND
6	AUDIO L (LEFT_IN_CD)
7	DSA_RST (SYS_RESET)
8	DOBM (DOBM_CD)
9	GND
10	SCLK (I^2S_BCLK_CD)
11	GND
12	WCLK (I^2S_WS_CD)
13	DATA (I^2S_DATA_CD)
14	GND
15	+12V
16	+5V
17	GND
18	DSA_ACK (DSA_ACK_CD)
19	DSA_STROBE (DSA_STR_CD)
20	GND
21	DSA_DATA (DSA_DATA_CD)
22	GND

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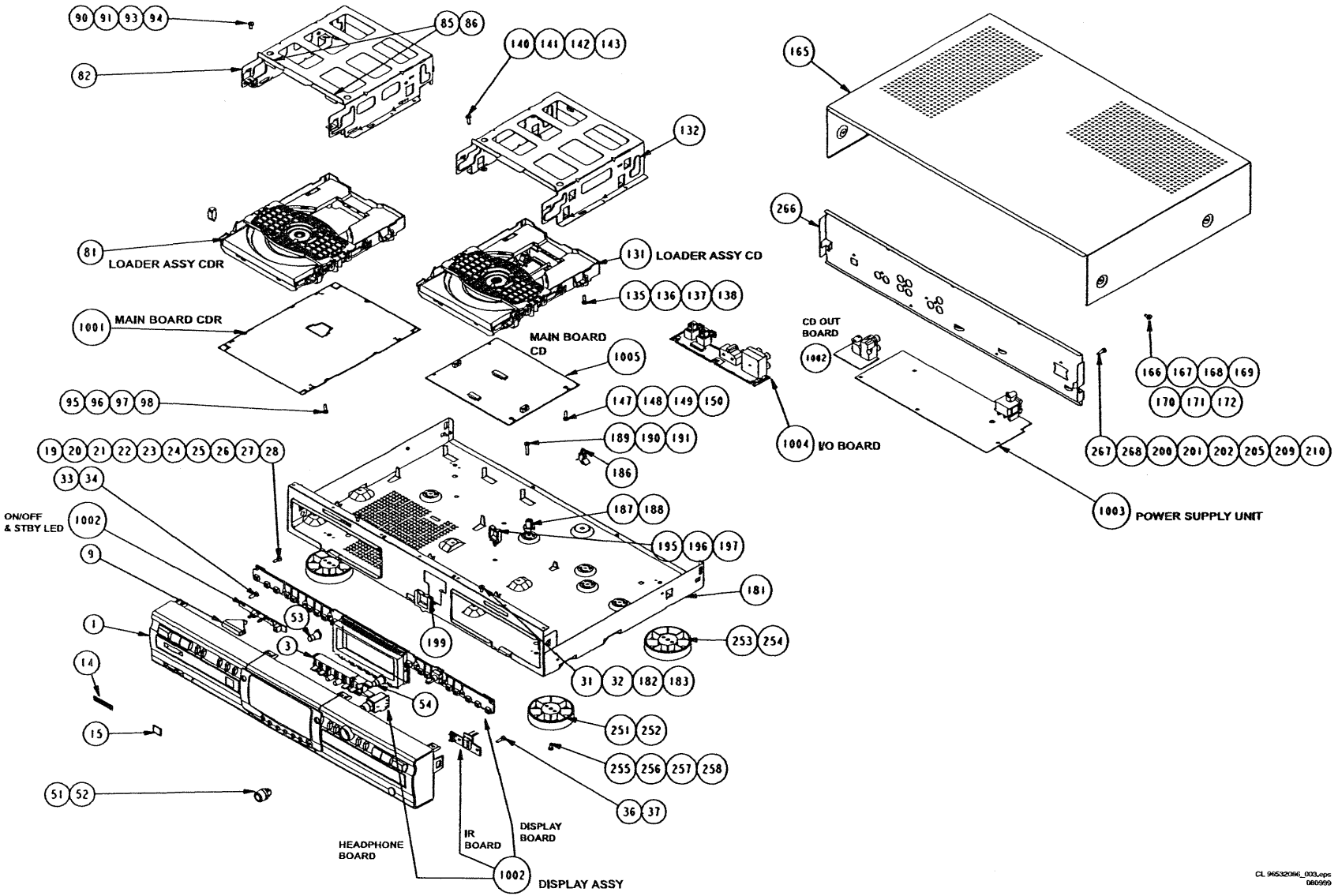
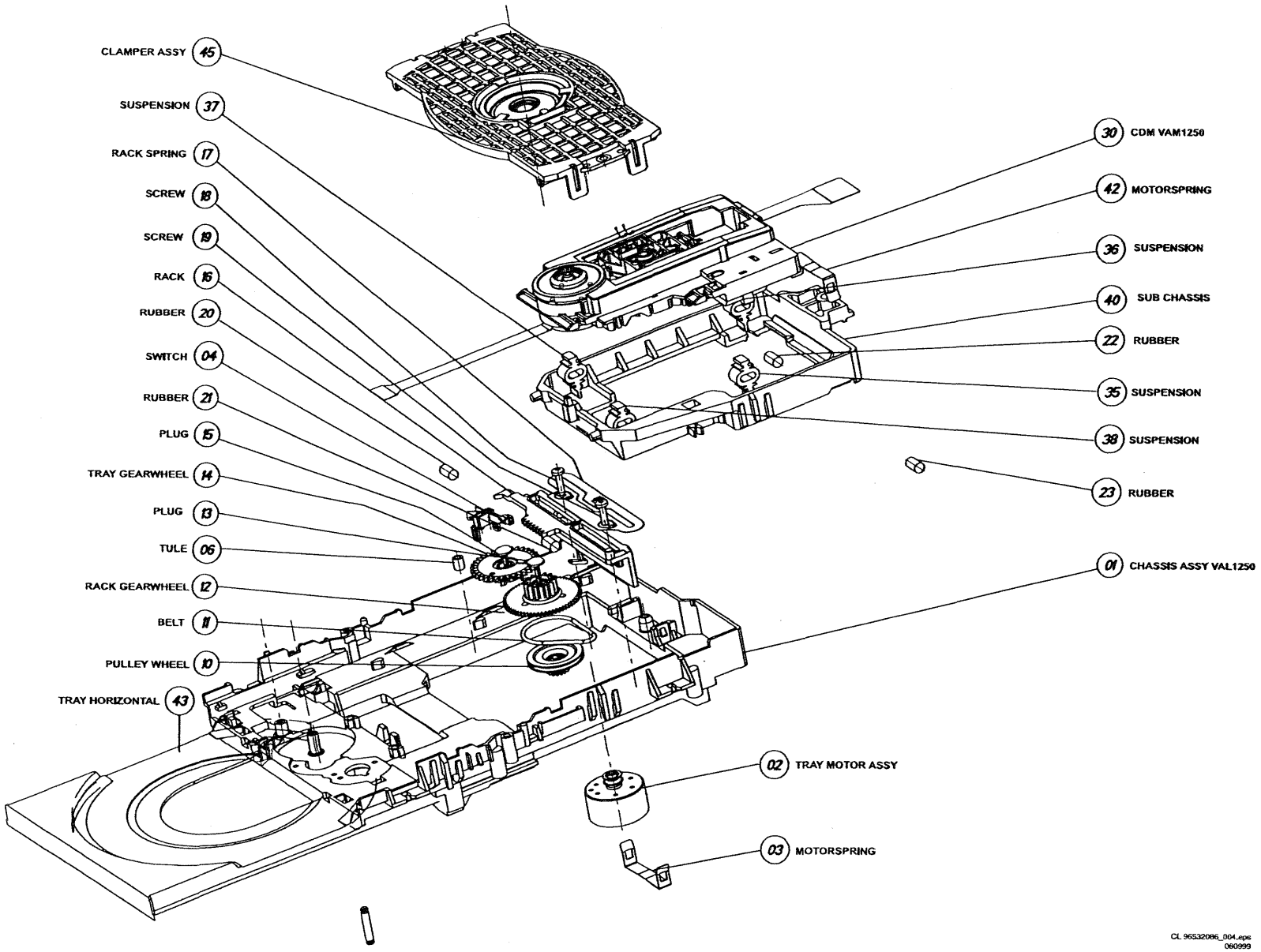
Exploded view CDR775

EXPLODED VIEW CDR775



Exploded view CD

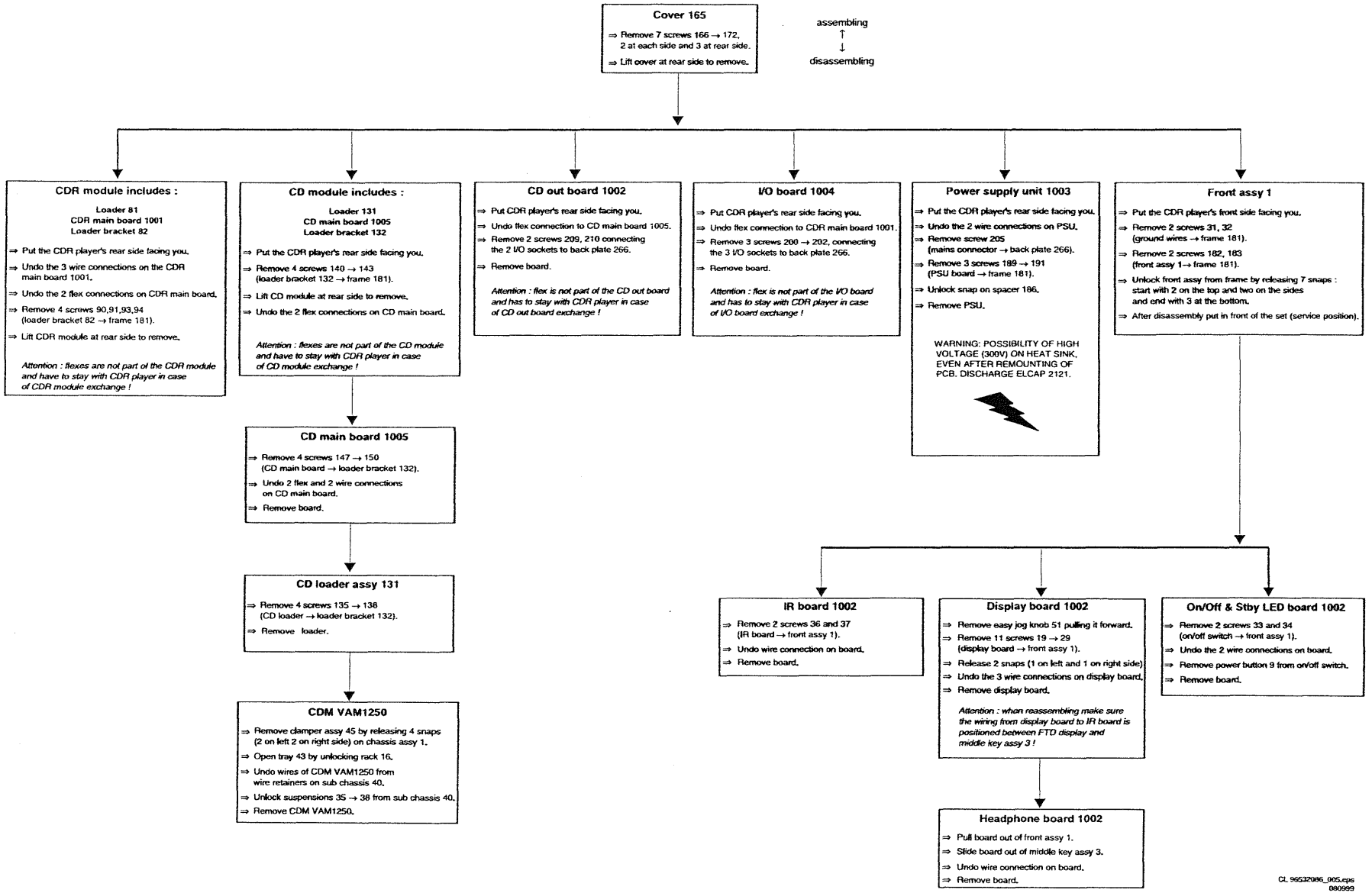
EXPLODED VIEW CD LOADER VAL1250



Dismantling 775

DISMANTLING INSTRUCTIONS CDR775

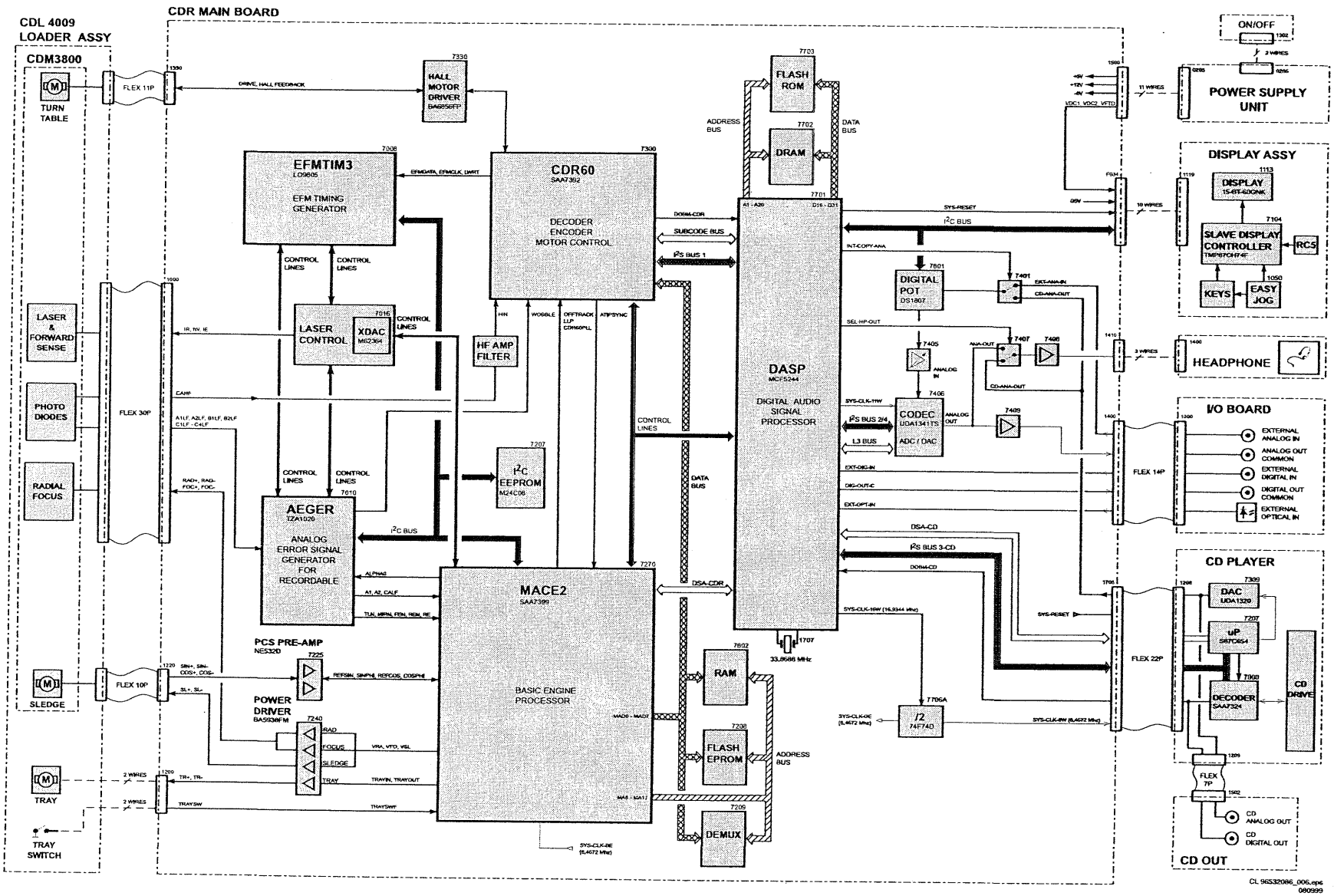
See exploded views for item numbers



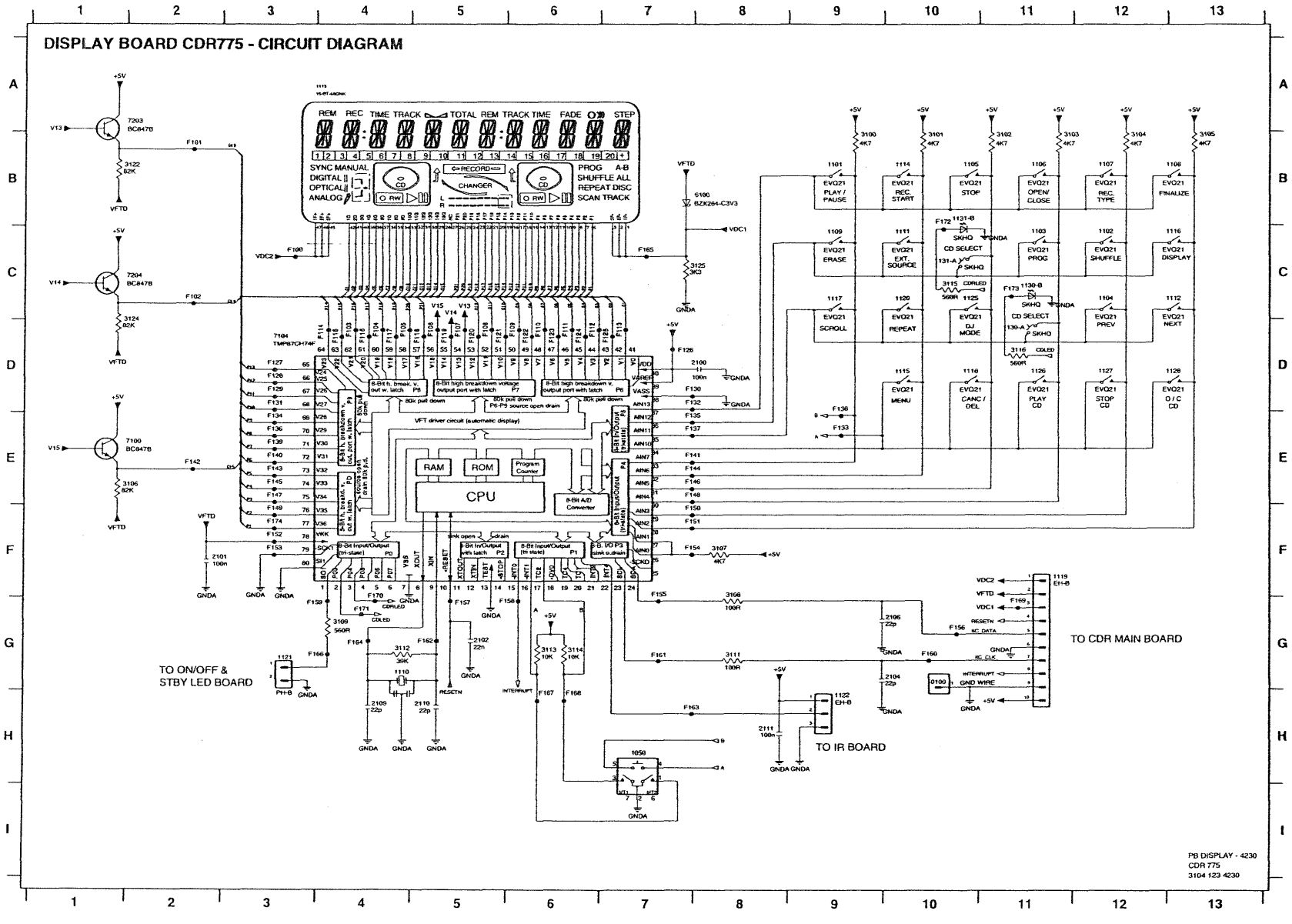
5. Electrical and circuit diagrams

Blockdiagram 775

OVERALL BLOCK DIAGRAM CDR775



Display 775


DISPLAY BOARD CDR775 - CIRCUIT DIAGRAM
REM REC TIME TRACK TOTAL REM TRACK TIME FADE STEP
SYNC MANUAL
DIGITAL
OPTICAL
ANALOG
PROG A-B
SHUFFLE ALL
REPEAT DISC
SCAN TRACK
CHANGER
RECORD
7203 BC847B
7204 BC847B
7100 BC847B
7104 TMP87CH74F
CPU
RAM
ROM
Program Counter
8-Bit A/D Converter
VFT driver circuit (automatic display)
EVO21 PLAY / PAUSE
EVO21 REC. START
EVO21 STOP
EVO21 OPEN/ CLOSE
EVO21 REC. TYPE
EVO21 FINALIZE
EVO21 ERASE
EVO21 EXT. SOURCE
EVO21 PROG
EVO21 SHUFFLE
EVO21 DISPLAY
EVO21 SCROLL
EVO21 REPEAT
EVO21 DJ MODE
EVO21 PREV
EVO21 NEXT
EVO21 MENU
EVO21 CANC / DEL
EVO21 PLAY CD
EVO21 STOP CD
EVO21 O / C CD
CD SELECT
EXT. SOURCE
CD SELECT
TO ON/OFF & STBY LED BOARD
TO CDR MAIN BOARD
TO IR BOARD
PB DISPLAY - 4230
CDR 775
3104 123 4230
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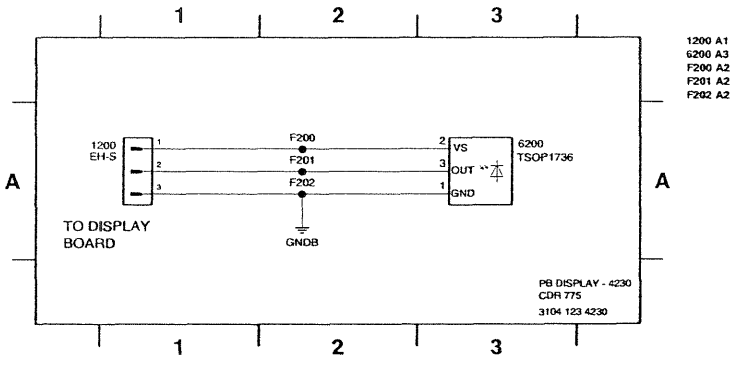
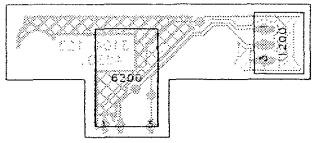
R on/off

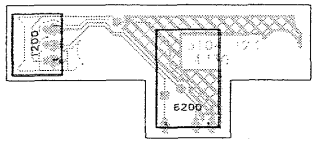
IR BOARD CDR775 - CIRCUIT DIAGRAM



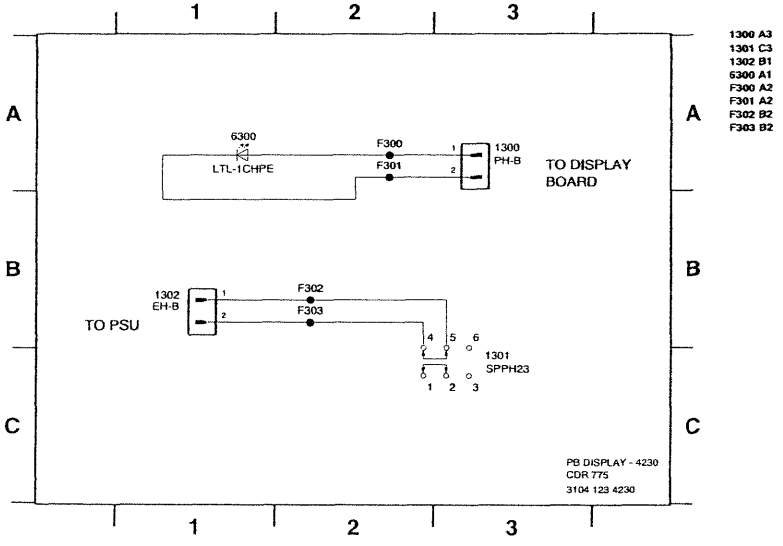
IR BOARD - FRONT VIEW



IR BOARD - BACK VIEW



ON/OFF & STBY LED BOARD CDR775 - CIRCUIT DIAGRAM



ON/OFF & STBY LED BOARD - FRONT VIEW

ON/OFF & STBY LED BOARD - BACK VIEW

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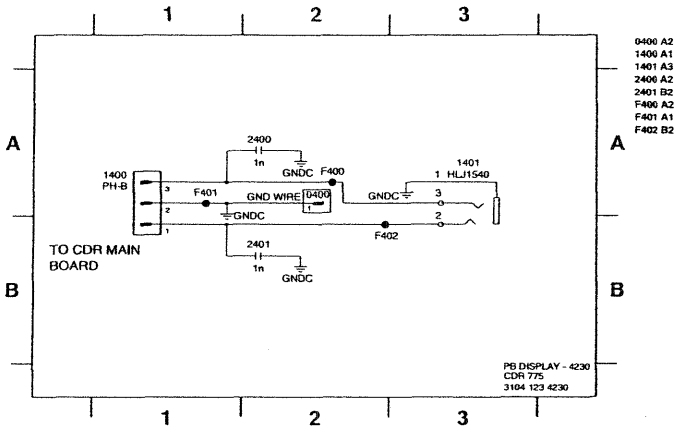
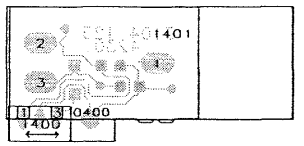
HPCD out

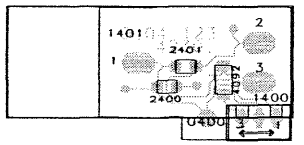
HEADPHONE BOARD CDR775 - CIRCUIT DIAGRAM



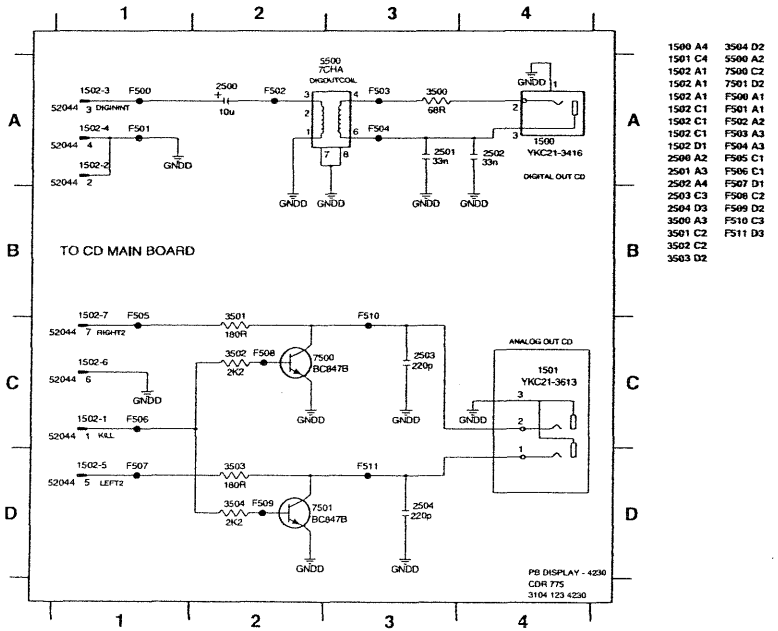
HEADPHONE BOARD - TOP VIEW



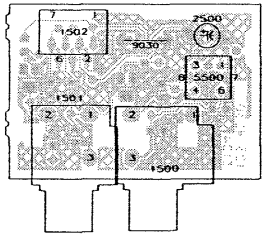
HEADPHONE BOARD - BOTTOM VIEW



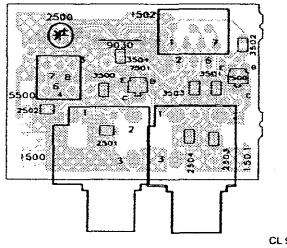
CD OUT BOARD CDR775 - CIRCUIT DIAGRAM



CD OUT BOARD - TOP VIEW



CD OUT BOARD - BOTTOM VIEW



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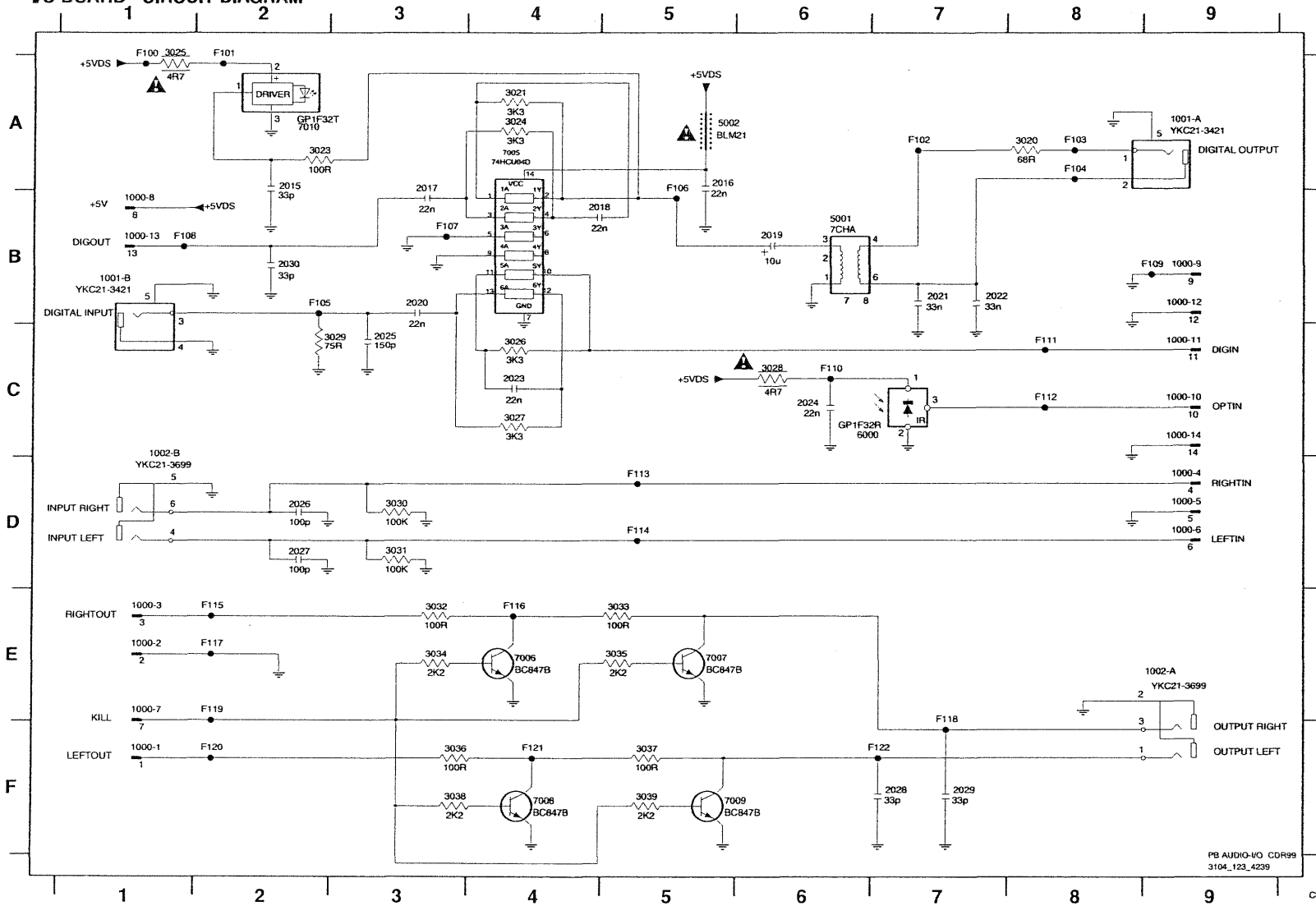
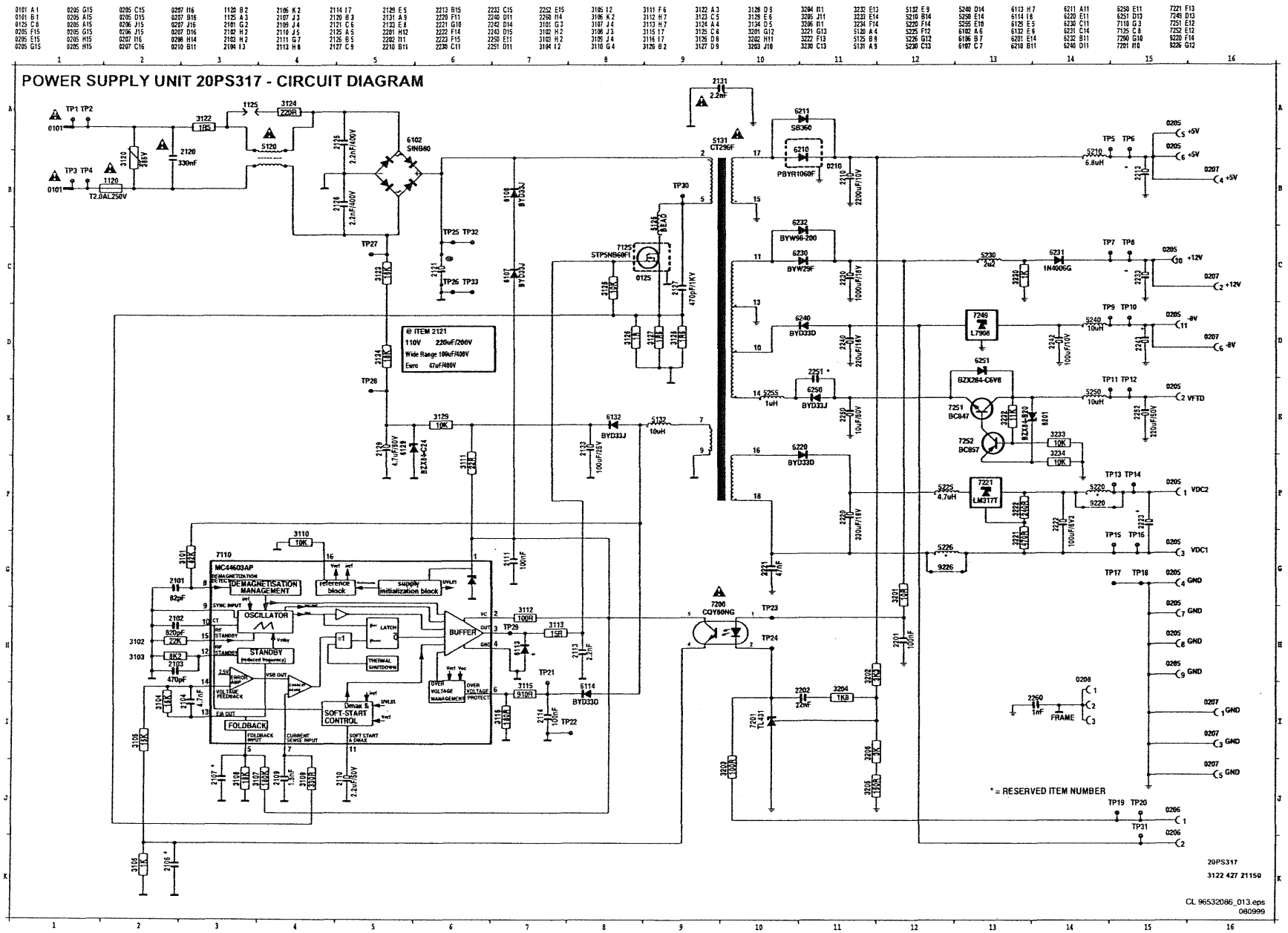
I/O board

I/O BOARD - CIRCUIT DIAGRAM

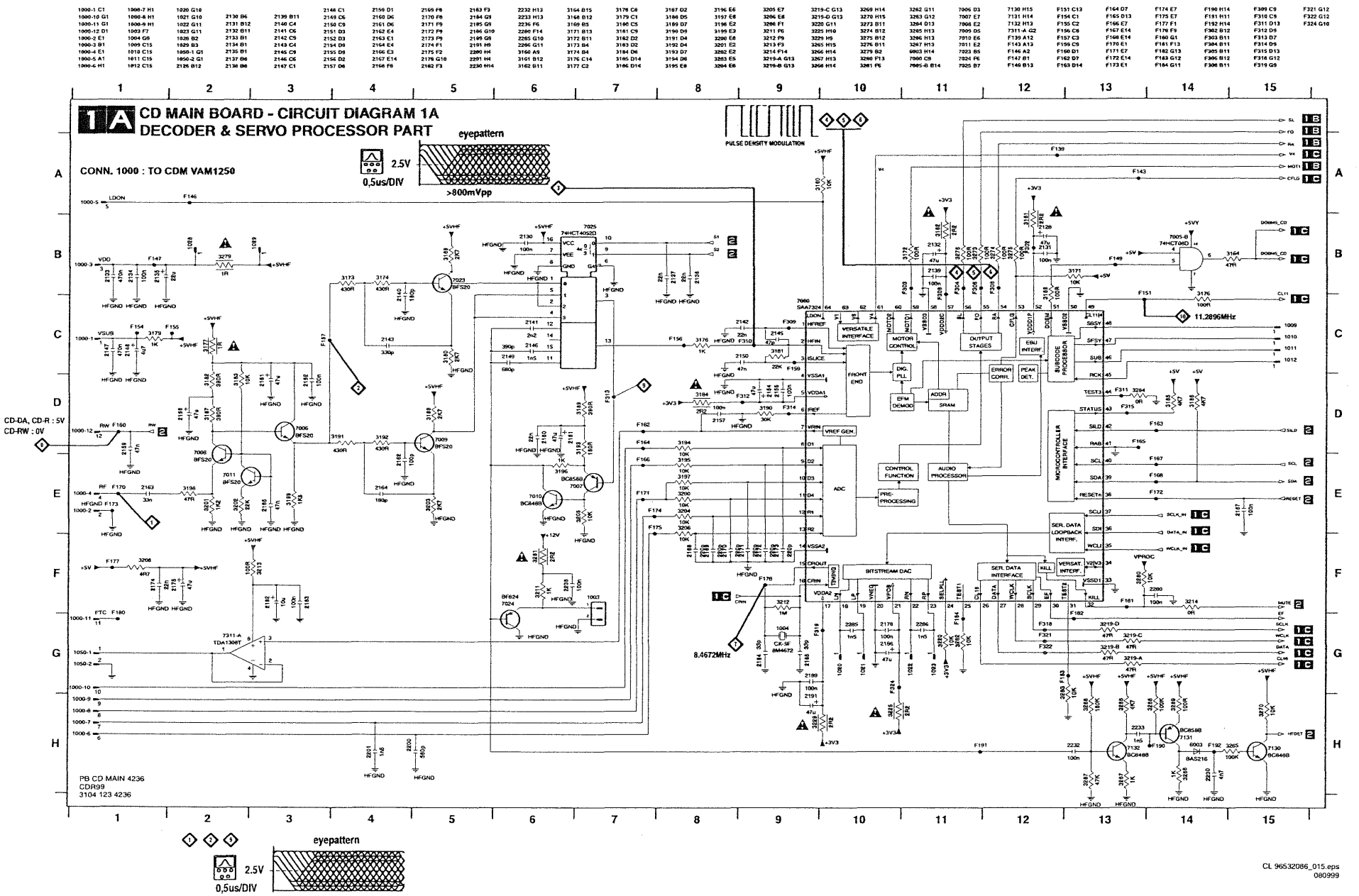


1000-1 F1
1000-10 C9
1000-11 C9
1000-12 B9
1000-13 B1
1000-14 C9
1000-2 E1
1000-3 E1
1000-4 D9
1000-5 D9
1000-6 D9
1000-7 E1
1000-8 B1
1000-9 B9
1001-A A9
1001-B B1
1002-A E9
1002-B D1
2015 A2
2016 A5
2017 B3
2018 B4
2019 B6
2020 B3
2021 B7
2022 B7
2023 C4
2024 C6
2025 C3
2026 D2
2027 D2
2028 F7
2029 F7
2030 B2
3020 A8
3021 A4
3023 A2
3024 A4
3025 A1
3026 C4
3027 C4
3028 C6
3029 C3
3030 D3
3031 D3
3032 E3
3033 E5
3034 E3
3035 E5
3036 F3
3037 F5
3038 F3
3039 F5
3999 F9
5001 B6
5002 A5
6000 C7
7005 A4
7006 E4
7007 E5
7008 F4
7009 F5
7010 A2

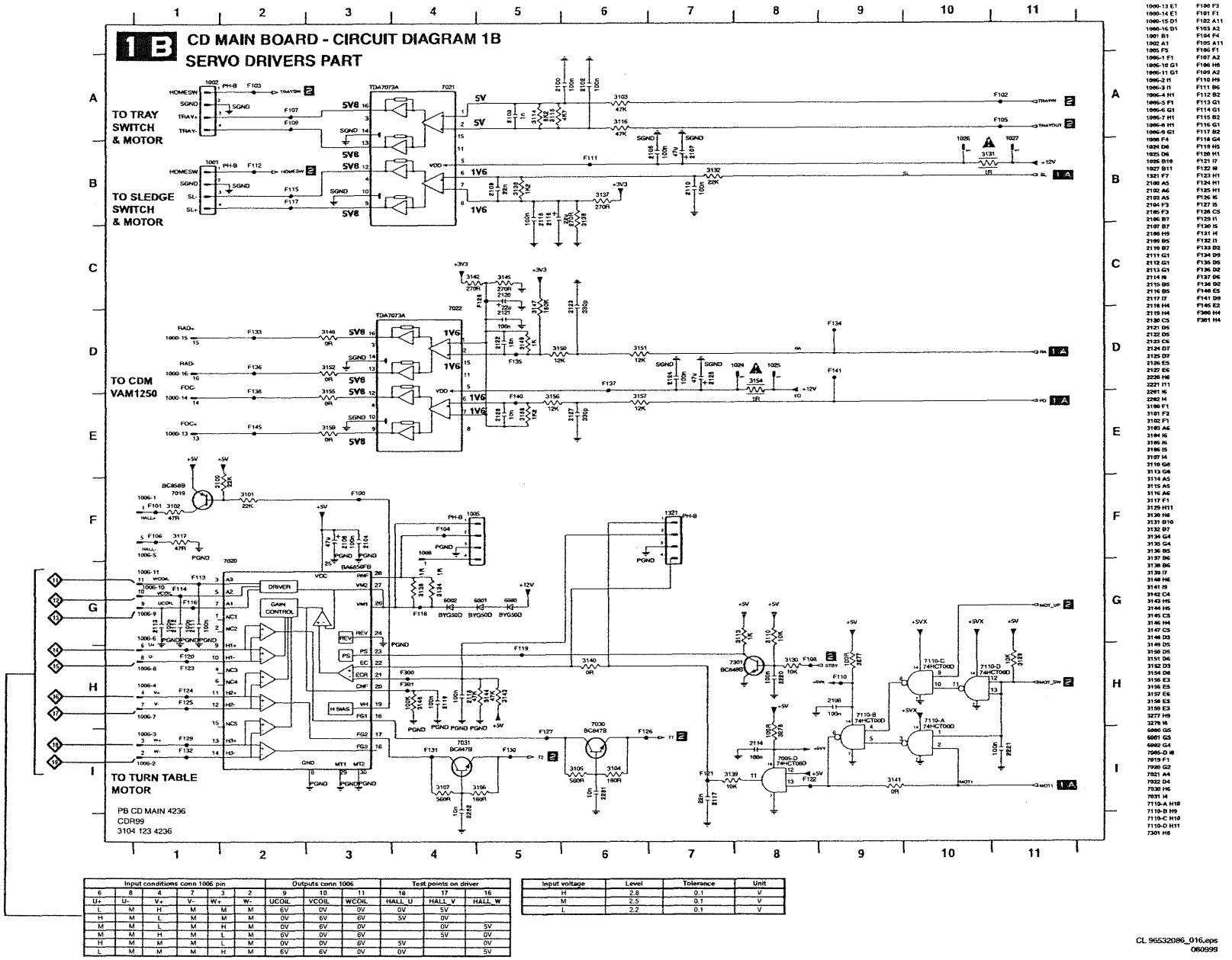
PSU 99


POWER SUPPLY UNIT 20PS317 - CIRCUIT DIAGRAM
MC44603AP
DEMAGNETISATION MANAGEMENT
OSCILLATOR
STANDBY
BUFFER
SOFT-START CONTROL
FOLDBACK
* = RESERVED ITEM NUMBER
20PS317
3122 427 21150
CL 96532086_013.eps
080999

CD Diagram 1A



CD diagram 1B

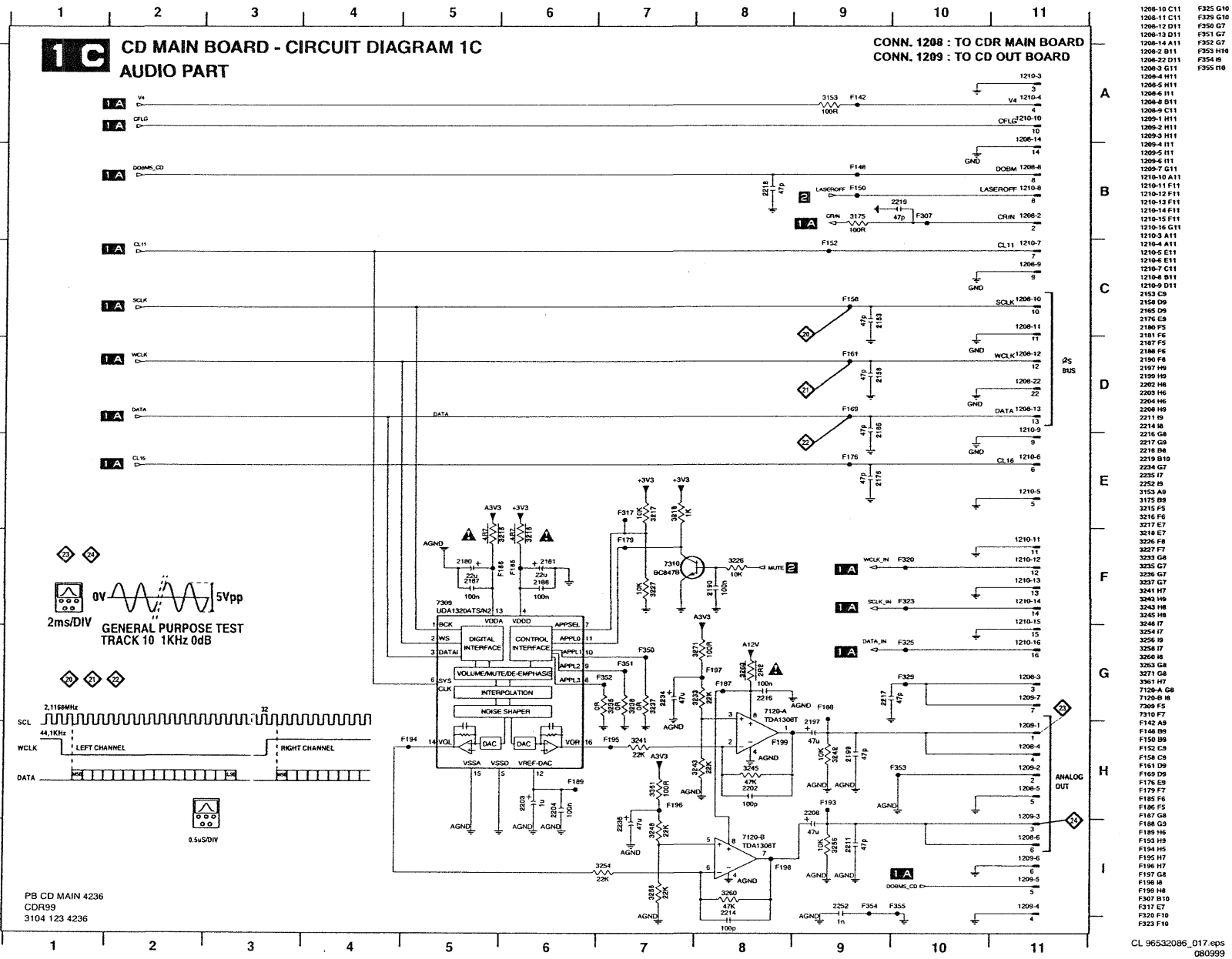


Input conditions conn 1006 pin						Outputs conn 1006			Test points on driver		
6	8	4	7	3	2	9	10	11	18	17	16
U+	U-	V+	V-	W+	W-	UCOIL	VCOIL	WCOIL	HALL_U	HALL_V	HALL_W
L	M	H	M	M	M	6V	0V	0V	0V	5V	
H	M	L	M	M	M	0V	6V	6V	5V	0V	
M	M	L	M	H	M	0V	6V	0V		0V	5V
M	M	H	M	L	M	6V	0V	6V		5V	0V
H	M	M	M	L	M	0V	0V	6V	5V		0V
L	M	M	M	H	M	6V	6V	0V	0V		5V

Input voltage	Level	Tolerance	Unit
H	2.8	0.1	V
M	2.5	0.1	V
L	2.2	0.1	V

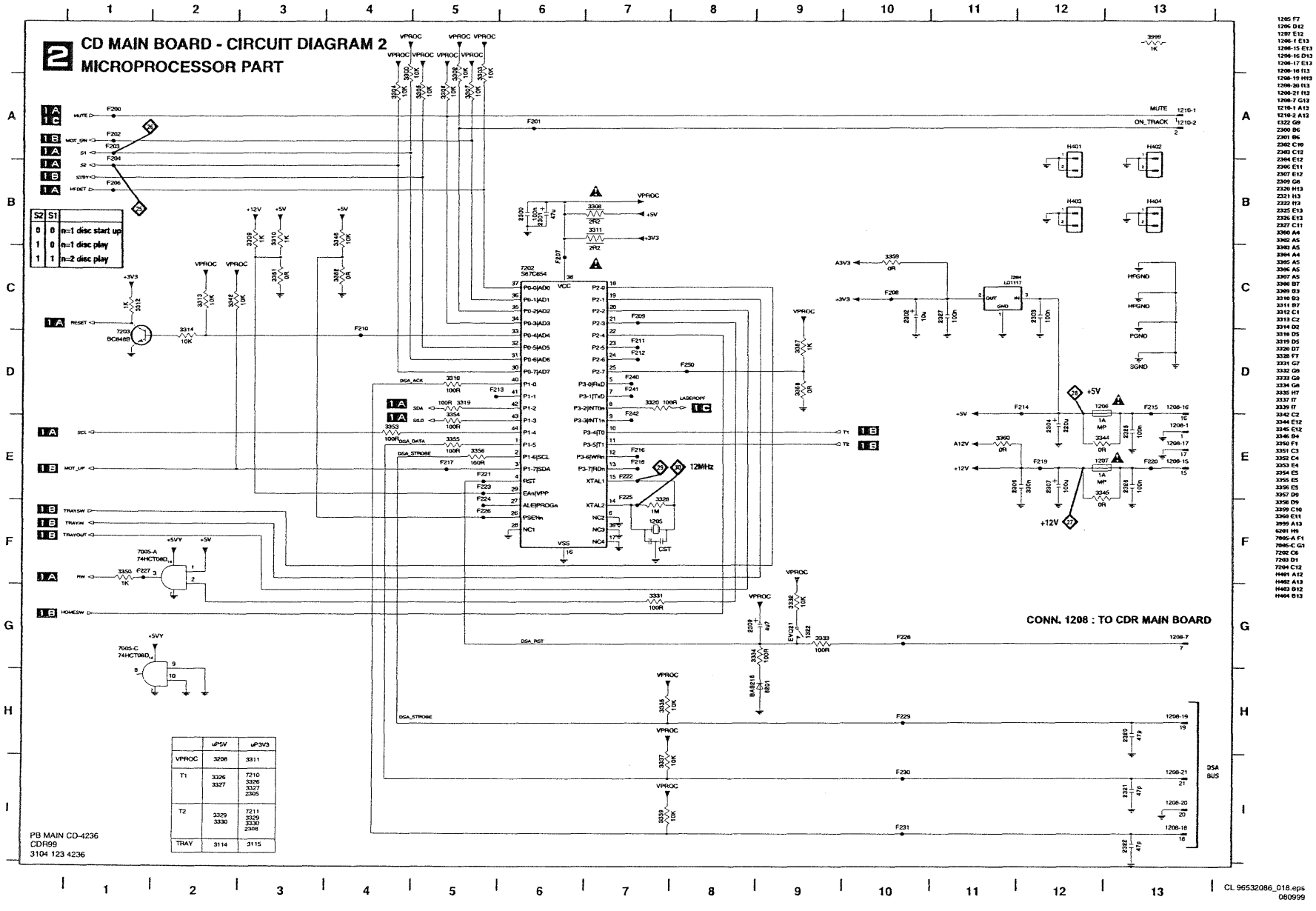
CL 96532086_016.eps
060999

CD diagram 1C



CL 96532086_017.eps
080999

CD diagram 2


2 CD MAIN BOARD - CIRCUIT DIAGRAM 2
MICROPROCESSOR PART
S2 S1
0 0 n=1 disc start up
1 0 n=1 disc play
1 1 n=2 disc play
CONN. 1208 : TO CDR MAIN BOARD
12MHz
DSA BUS
PB MAIN CD-4236
CDR99
3104 123 4236
CL 96532086_018.eps
080999